Compact, 800 mA, 3 MHz, Step-Down DC-to-DC Converter

Data Sheet

ADP2138/ADP2139

FEATURES

- Input voltage: 2.3 V to 5.5 V
- Peak efficiency: 95%
- 3 MHz fixed frequency operation
- Typical quiescent current: 24 µA
- Very small solution size
- 6-lead, 1 mm × 1.5 mm WLCSP package
- Fast load and line transient response
- 100% duty cycle low dropout mode
- Internal synchronous rectifier, compensation, and soft start
- Current overload and thermal shutdown protections
- Ultralow shutdown current: 0.2 µA (typical)
- Forced PWM and automatic PWM/PSM modes
- Supported by ADIsimPower™ design tool

APPLICATIONS

- PDAs and palmtop computers
- Wireless handsets
- Digital audio, portable media players
- Digital cameras, GPS navigation units

GENERAL DESCRIPTION

The ADP2138 and ADP2139 are high efficiency, low quiescent current, synchronous step-down dc-to-dc converters. The ADP2139 has the additional feature of an internal discharge switch. The total solution requires only three tiny external components. When the MODE pin is set high, the buck regulator operates in forced PWM mode, which provides low peak-to-peak ripple for power supply noise sensitive loads at the expense of light load efficiency. When the MODE pin is set low, the buck regulator automatically switches operating modes, depending on the load current level. At higher output loads, the buck regulator operates in PWM mode. When the load current falls below a predefined threshold, the regulator operates in power save mode (PSM), improving light load efficiency.

The ADP2138/ADP2139 operate on input voltages of 2.3 V to 5.5 V, which allows for single lithium or lithium polymer cell, multiple alkaline or NiMH cell, PCMCIA, USB, and other standard power sources. The maximum load current of 800 mA is achievable across the input voltage range.

The ADP2138/ADP2139 are available in fixed output voltages of 3.3 V, 3.0 V, 2.8 V, 2.5 V, 1.8 V, 1.5 V, 1.2 V, 1.0 V, and 0.8 V. All versions include an internal power switch and synchronous rectifier for minimal external part count and high efficiency. The ADP2138/ADP2139 have internal soft start and they are internally compensated. During logic controlled shutdown, the input is disconnected from the output and the ADP2138/ADP2139 draw 0.2 µA (typical) from the input source.

Other key features include undervoltage lockout to prevent deep battery discharge, and soft start to prevent input current overshoot at startup. The ADP2138/ADP2139 are available in a 6-ball wafer level chip scale package (WLCSP).

TYPICAL APPLICATIONS CIRCUIT

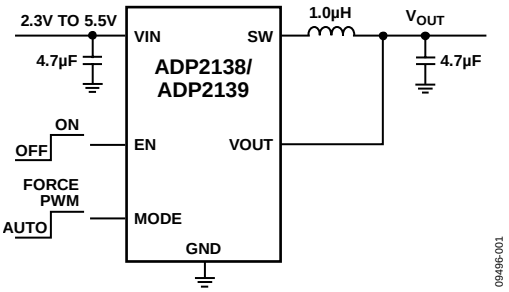

Figure 1.

Rev. C

Document Feedback

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4/11—Rev. 0 to Rev. A

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1/11—Revision 0: Initial Version

SPECIFICATIONS

V_{IN} = 3.6 V, V_{OUT} = 0.8 V − 3.3 V, T_J = −40°C to +125°C for minimum/maximum specifications, and T_A = 25°C for typical specifications, unless otherwise noted. All limits at temperature extremes are guaranteed via correlation using standard statistical quality control (SQC).

Table 1.

Parameter	Test Conditions/Comments	Min	Typ	Max	Unit
INPUT CHARACTERISTICS					
Input Voltage Range		2.3		5.5	V
Undervoltage Lockout Threshold	V_{IN} rising			2.3	V
	V_{IN} falling	2.00	2.15	2.25	V
OUTPUT CHARACTERISTICS					
Output Voltage Accuracy	PWM mode	−2		+2	%
Line Regulation	V_{IN} = 2.3 V to 5.5 V, PWM mode		0.25		%/V
Load Regulation	I_{LOAD} = 0 mA − 800 mA		−0.95		%/A
PWM TO POWER SAVE MODE CURRENT THRESHOLD			100		mA
INPUT CURRENT CHARACTERISTICS					
DC Operating Current	I_{LOAD} = 0 mA, device not switching		23	30	µA
Shutdown Current	EN = 0 V, $T_A = T_J$ = −40°C to +85°C		0.2	1.0	µA
SW CHARACTERISTICS					
SW On Resistance	PFET		155	240	mΩ
	NFET		115	200	mΩ
Current Limit	PFET switch peak current limit	1100	1500	1650	mA
Discharge Switch (ADP2139)			100		Ω
ENABLE AND MODE CHARACTERISTICS					
Input High Threshold		1.2			V
Input Low Threshold				0.4	V
Input Leakage Current	EN/MODE = 0 V (min), 3.6 V (max)	−1	0	+1	µA
OSCILLATOR FREQUENCY		2.6	3.0	3.4	MHz
START-UP TIME			250		µs
THERMAL CHARACTERISTICS					
Thermal Shutdown Threshold			150		°C
Thermal Shutdown Hysteresis			20		°C

INPUT AND OUTPUT CAPACITOR, RECOMMENDED SPECIFICATIONS

T_A = −40°C to +125°C, unless otherwise specified. All limits at temperature extremes are guaranteed via correlation using standard statistical quality control (SQC).

Table 2.

Parameter	Symbol	Min	Typ	Max	Unit
MINIMUM INPUT AND OUTPUT CAPACITANCE	C_{MIN}	4.7			µF
CAPACITOR ESR	R_{ESR}	0.001		1	Ω

ABSOLUTE MAXIMUM RATINGS

Table 3.

Parameter	Rating
VIN, EN, MODE	−0.4 V to +6.5 V
VOUT, SW to GND	−1.0 V to (V_{IN} + 0.2 V)
Temperature Range	
Operating Ambient	−40°C to +85°C
Operating Junction	−40°C to +125°C
Storage Temperature	−65°C to +150°C
Lead Temperature Range	−65°C to +150°C
Soldering (10 sec)	300°C
Vapor Phase (60 sec)	215°C
Infrared (15 sec)	220°C
ESD Model	
Human Body	±1500 V
Charged Device	±500 V
Machine	±100 V

Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only; functional operation of the device at these or any other conditions above those indicated in the operational section of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

THERMAL DATA

Absolute maximum ratings apply individually only, not in combination.

ADP2138/ADP2139 can be damaged when the junction temperature limits are exceeded. Monitoring ambient temperature does not guarantee that the junction temperature (T_J) is within the specified temperature limits. In applications with high power dissipation and poor thermal resistance, the maximum ambient temperature may need to be derated. In applications with moderate power dissipation and low printed circuit board (PCB) thermal resistance, the maximum ambient temperature can exceed the maximum limit for as long as the junction temperature is within specification limits. The junction temperature (T_J) of the device is dependent on the ambient temperature (T_A), the power dissipation of the device (P_D), and the junction-to-ambient thermal resistance of the package (θ_{JA}). Maximum junction temperature (T_J) is calculated from the ambient temperature (T_A) and power dissipation (P_D) using the formula

$$T_J = T_A + (P_D \times \theta_{JA})$$

Junction-to-ambient thermal resistance (θ_{JA}) of the package is based on modeling and calculation using a 4-layer board. The junction-to-ambient thermal resistance is highly dependent on the application and board layout. In applications where high maximum power dissipation exists, close attention to thermal board design is required. The value of θ_{JA} may vary, depending on PCB material, layout, and environmental conditions. The specified values of θ_{JA} are based on a 4-layer, 4 in. × 3 in., circuit board. Refer to JEDEC JESD 51-9 for detailed information pertaining to board construction. For additional information, see AN-617 Application Note, *MicroCSP™ Wafer Level Chip Scale Package*.

Ψ_{JB} is the junction-to-board thermal characterization parameter measured in units of °C/W. Ψ_{JB} of the package is based on modeling and calculation using a 4-layer board. The JESD51-12, *Guidelines for Reporting and Using Package Thermal Information*, states that thermal characterization parameters are not the same as thermal resistances. Ψ_{JB} measures the component power flowing through multiple thermal paths rather than through a single path, which is the procedure for measuring thermal resistance, θ_{JB}. Therefore, Ψ_{JB} thermal paths include convection from the top of the package as well as radiation from the package; factors that make Ψ_{JB} more useful in real-world applications than θ_{JB}. Maximum junction temperature (T_J) is calculated from the board temperature (T_B) and power dissipation (P_D) using the formula

$$T_J = T_B + (P_D \times \Psi_{JB})$$

Refer to JEDEC JESD51-8 and JESD51-12 for more detailed information about Ψ_{JB}.

THERMAL RESISTANCE

θ_{JA} and Ψ_{JB} are specified for the worst-case conditions, that is, a device soldered in a circuit board for surface-mount packages.

Table 4. Thermal Resistance

Package Type	θ_{JA}	Ψ_{JB}	Unit
6-Ball WLCSP	170	80	°C/W

ESD CAUTION

ESD (electrostatic discharge) sensitive device. Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

PIN CONFIGURATION AND FUNCTION DESCRIPTIONS

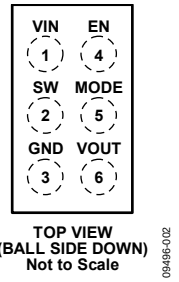

Figure 2. Pin Configuration (Top View)

Table 5. Pin Function Descriptions

Pin No.	Mnemonic	Description
1	VIN	Power Source Input. VIN is the source of the PFET high-side switch. Bypass VIN to GND with a 4.7 µF or greater capacitor as close to the ADP2138/ADP2139 as possible.
2	SW	Switch Node Output. SW is the drain of the P-channel MOSFET switch and N-channel synchronous rectifier. Connect the output LC filter between SW and the output voltage.
3	GND	Ground. Connect the input and output capacitors to GND.
4	EN	Buck Activation. To turn on the buck, set EN to high. To turn off the buck, set EN to low.
5	MODE	Mode Input. Drive the MODE pin high for the operating mode to force continuous PWM switching. Drive the MODE pin low to allow automatic PWM/PSM operating mode.
6	VOUT	Output Voltage Sensing Input.

TYPICAL PERFORMANCE CHARACTERISTICS

V_{IN} = 3.6 V, T_A = 25°C, V_{EN} = V_{IN}, unless otherwise noted.

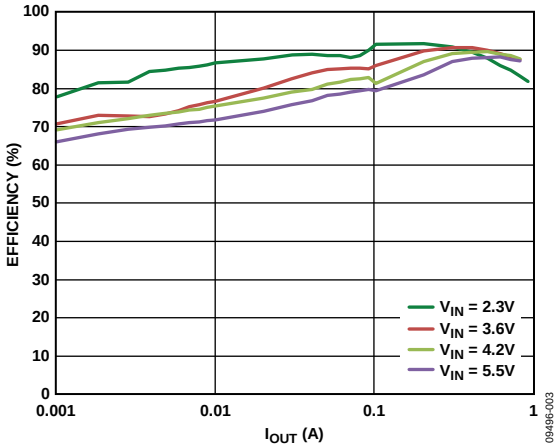

Figure 3. Efficiency vs. Load Current, Across Input Voltage, V_{OUT} = 1.8 V, PSM Mode

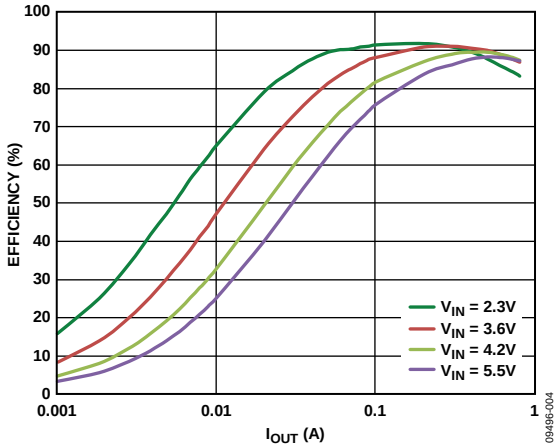

Figure 4. Efficiency vs. Load Current, Across Input Voltage, V_{OUT} = 1.8 V, PWM Mode

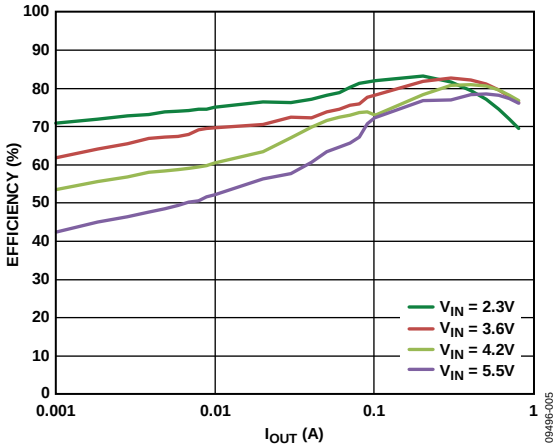

Figure 5. Efficiency vs. Load Current, Across Input Voltage, V_{OUT} = 0.8 V, PSM Mode

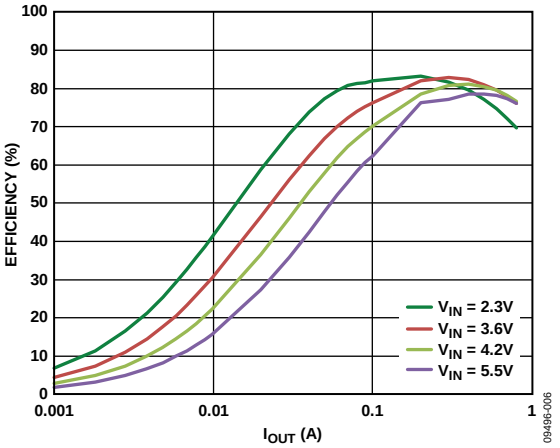

Figure 6. Efficiency vs. Load Current, Across Input Voltage, V_{OUT} = 0.8 V, PWM Mode

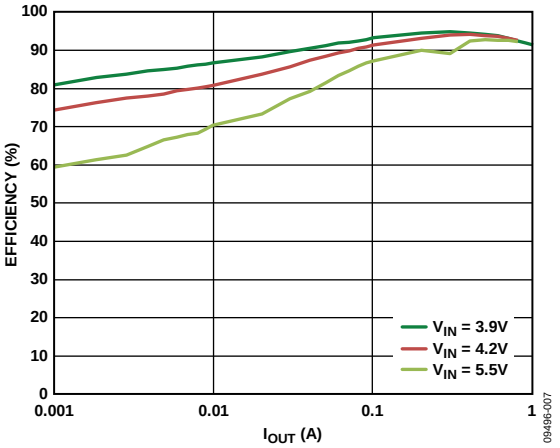

Figure 7. Efficiency vs. Load Current, Across Input Voltage, V_{OUT} = 3.3 V, PSM Mode

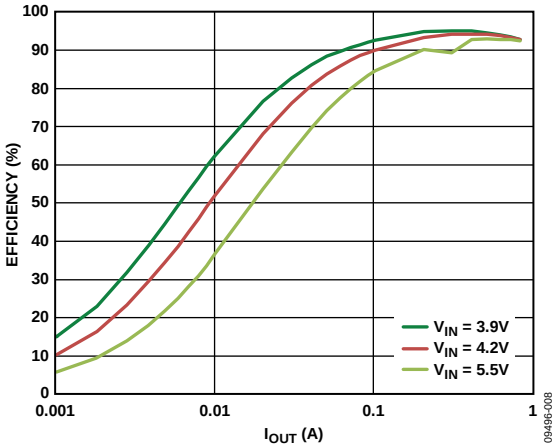

Figure 8. Efficiency vs. Load Current, Across Input Voltage, V_{OUT} = 3.3 V, PWM Mode

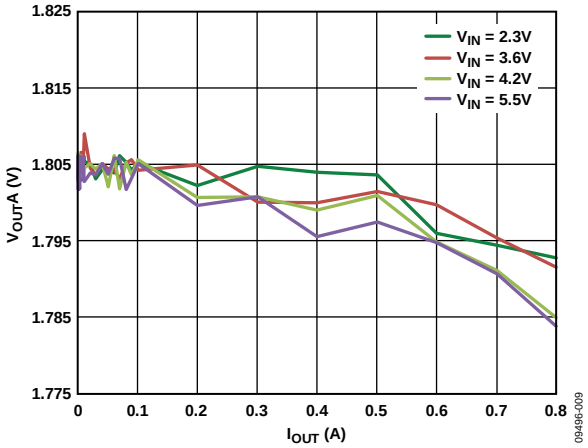

Figure 9. Load Regulation Across Input Voltage, V_{OUT} = 1.8 V, PWM Mode

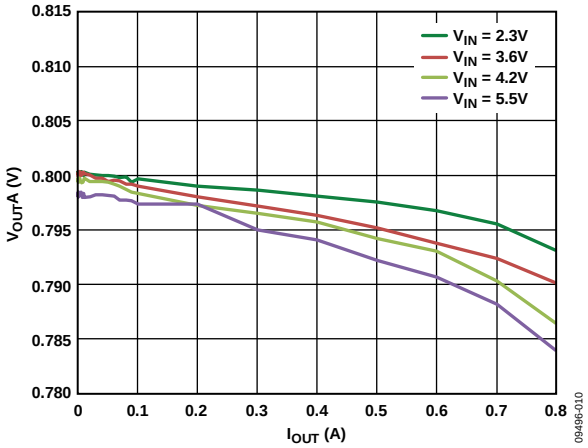

Figure 10. Load Regulation Across Input Voltage, V_{OUT} = 0.8 V, PWM Mode

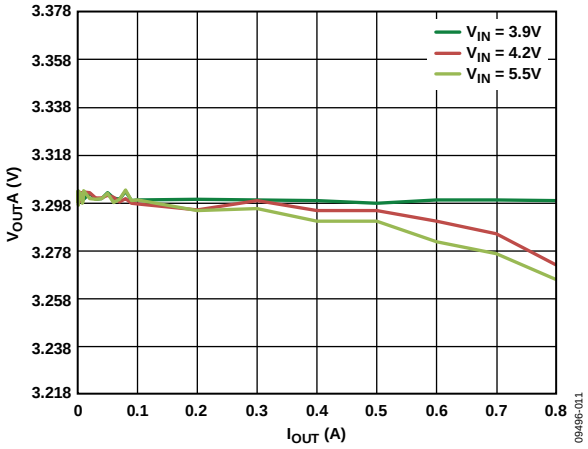

Figure 11. Load Regulation Across Input Voltage, V_{OUT} = 3.3 V, PWM Mode

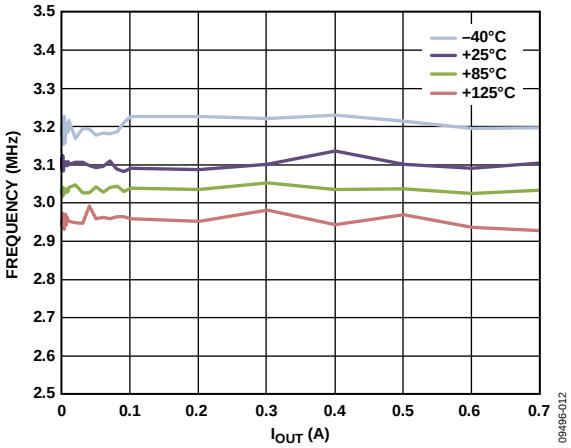

Figure 12. Frequency vs. Output Current, Across Temperature, V_{OUT} = 1.8 V, PWM Mode

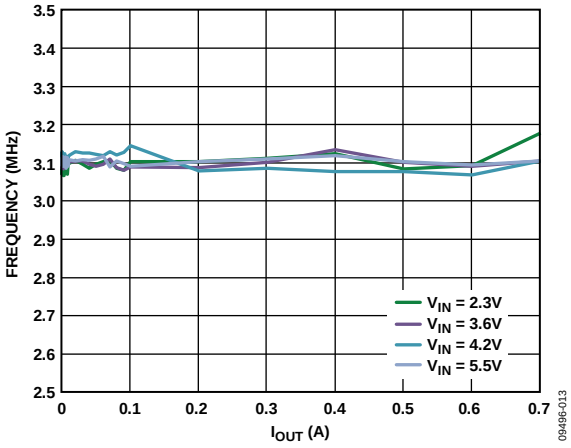

Figure 13. Frequency vs. Output Current, Across Supply Voltage, V_{OUT} = 1.8 V

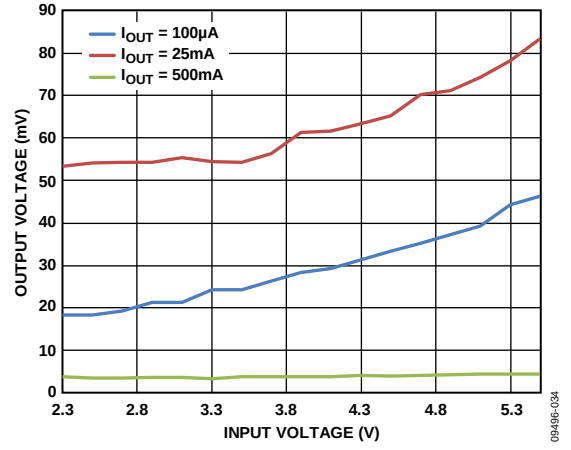

Figure 14. Output Voltage Ripple vs. Input Voltage, Across Output Current, V_{OUT} = 1.8 V

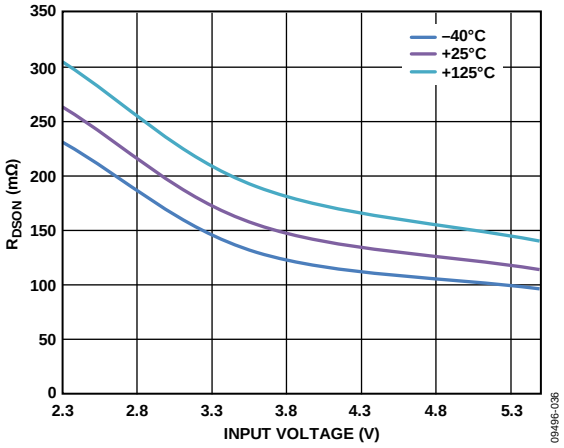

Figure 15. R_{DSON} PFET vs. Input Voltage, Across Temperature

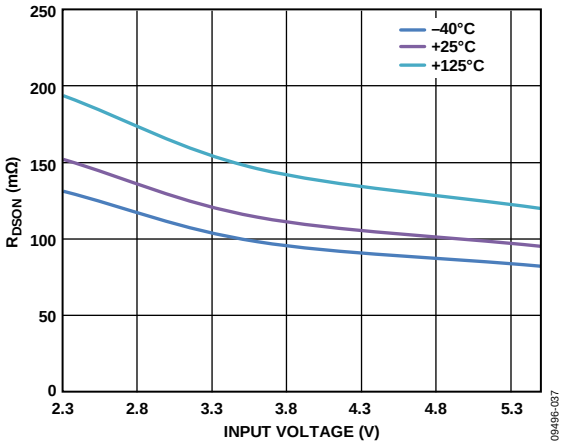

Figure 16. R_{DSON} NFET vs. Input Voltage, Across Temperature

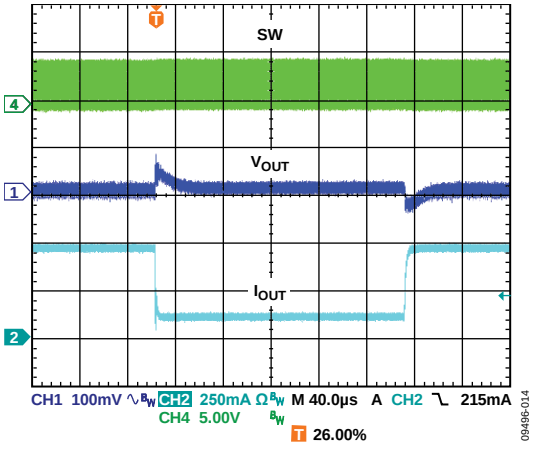

Figure 17. Response to Load Transient, 150 mA to 500 mA, V_{OUT} = 1.8 V, PWM Mode

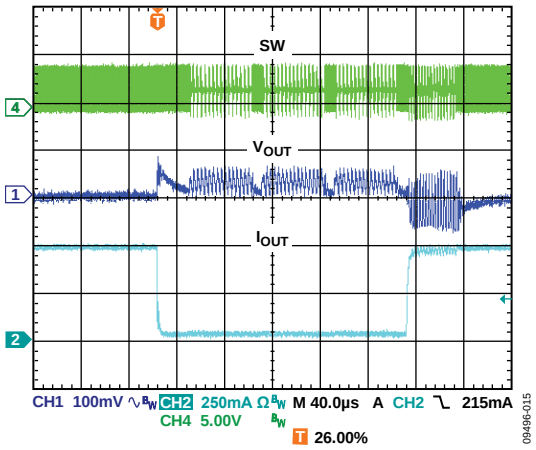

Figure 18. Response to Load Transient, 50 mA to 500 mA, V_{OUT} = 1.8 V, Automatic Mode

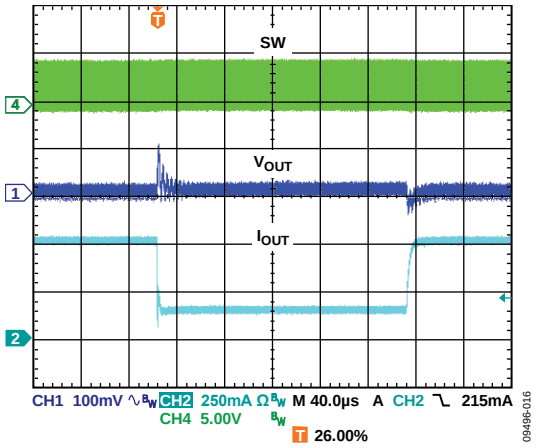

Figure 19. Response to Load Transient, 150 mA to 500 mA, V_{OUT} = 0.8 V, PWM Mode

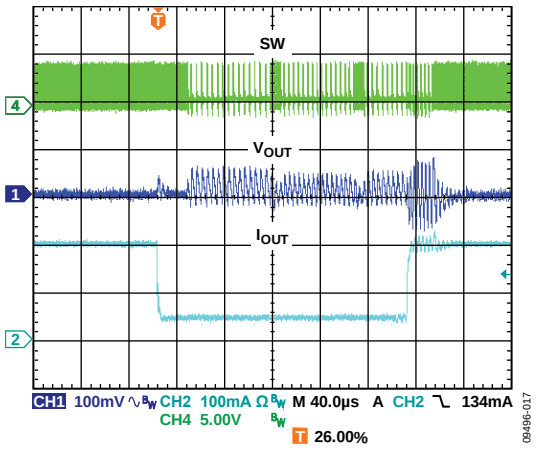

Figure 20. Response to Load Transient, 50 mA to 200 mA, V_{OUT} = 0.8 V, Automatic Mode

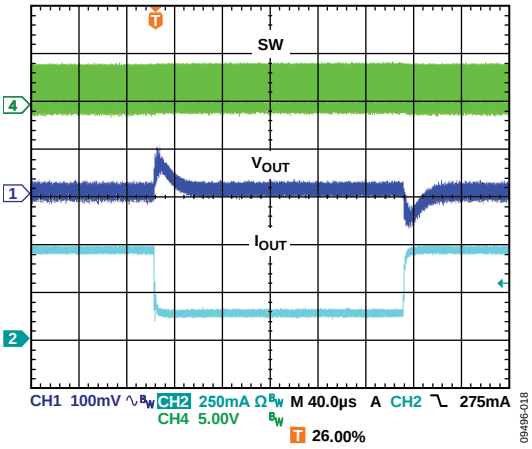

Figure 21. Response to Load Transient, 150 mA to 500 mA, V_{OUT} = 3.3 V, PWM Mode

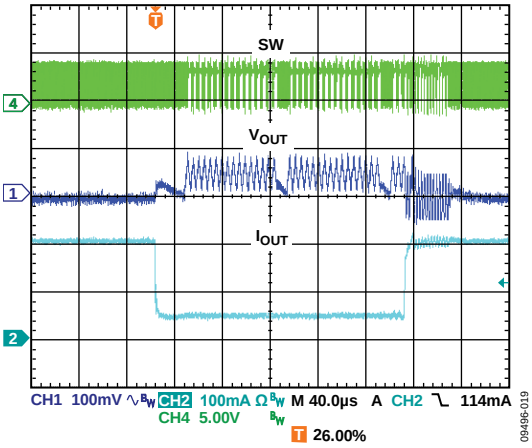

Figure 22. Response to Load Transient, 50 mA to 200 mA, V_{OUT} = 3.3 V, Automatic Mode

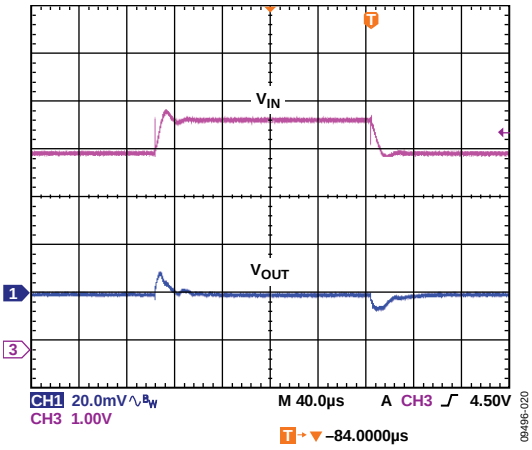

Figure 23. Response to Line Transient, V_{OUT} = 3.3 V, V_{IN} = 4.0 V to 4.8 V, PWM Mode

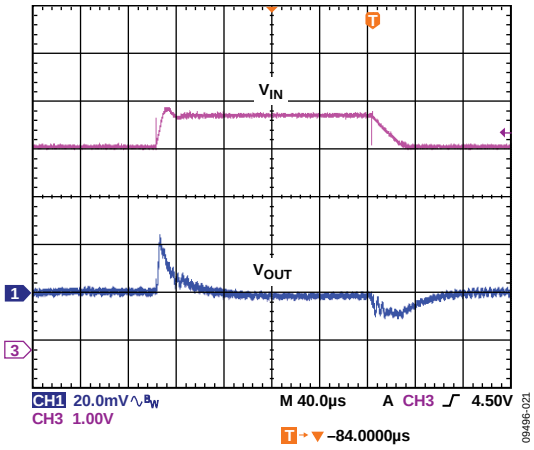

Figure 24. Response to Line Transient, V_{OUT} = 0.8 V, V_{IN} = 4.0 V to 4.8 V, PWM Mode

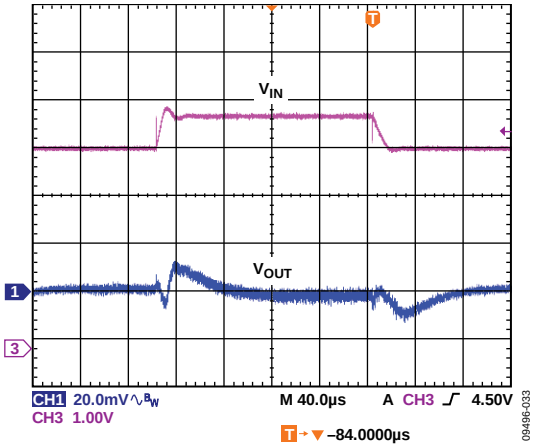

Figure 25. Response to Line Transient, V_{OUT} = 1.8 V, V_{IN} = 4.0 V to 4.8 V, PWM Mode

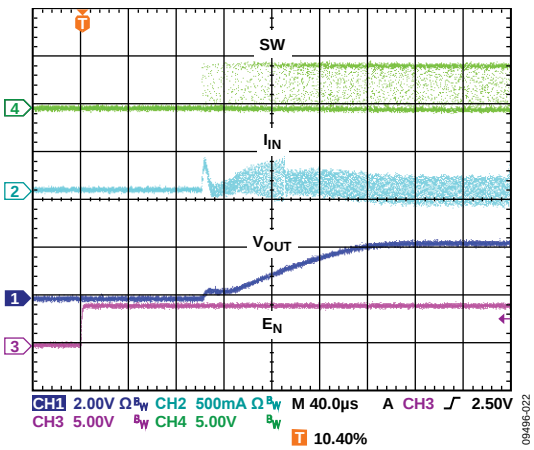

Figure 26. Startup, V_{OUT} = 1.8 V, I_{OUT} = 10 mA

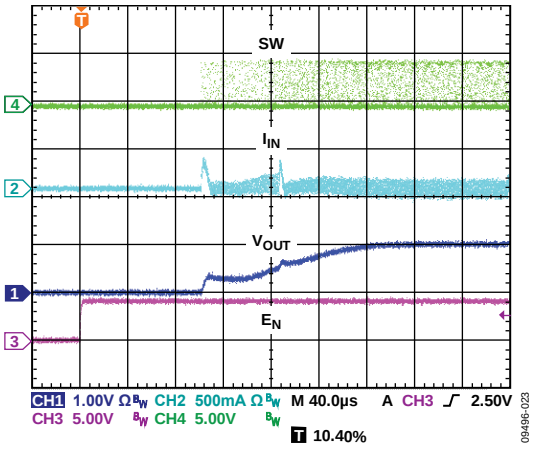

Figure 27. Startup, V_{OUT} = 0.8 V, I_{OUT} = 10 mA

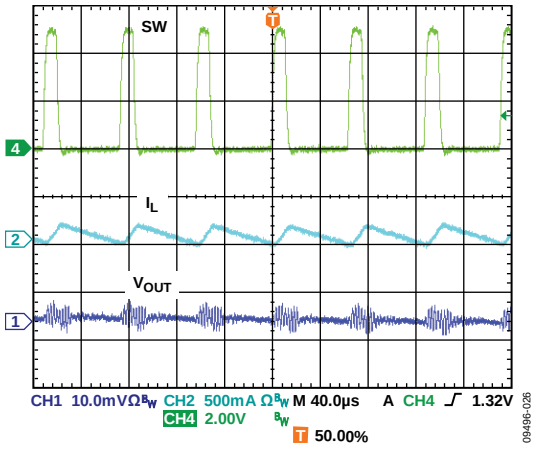

Figure 30. Typical Waveform, V_{OUT} = 1.8 V, PWM Mode, I_{OUT} = 200 mA

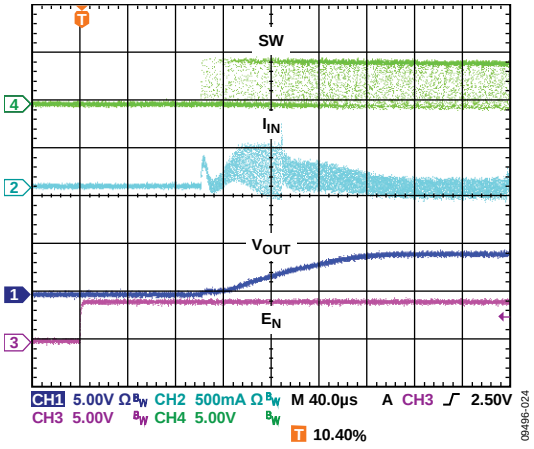

Figure 28. Startup, V_{OUT} = 3.3 V, I_{OUT} = 10 mA

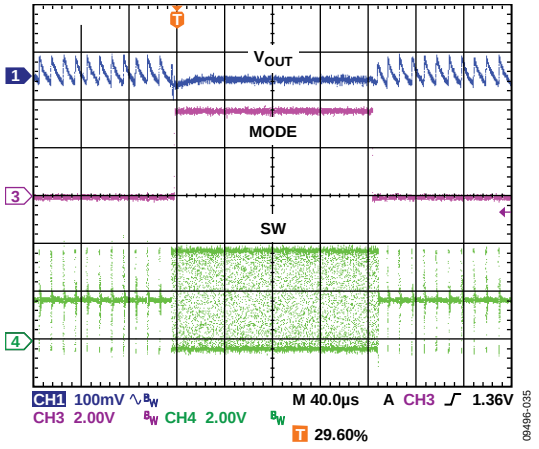

Figure 31. Mode Transition from PSM to PWM to PSM, V_{OUT} = 1.8 V

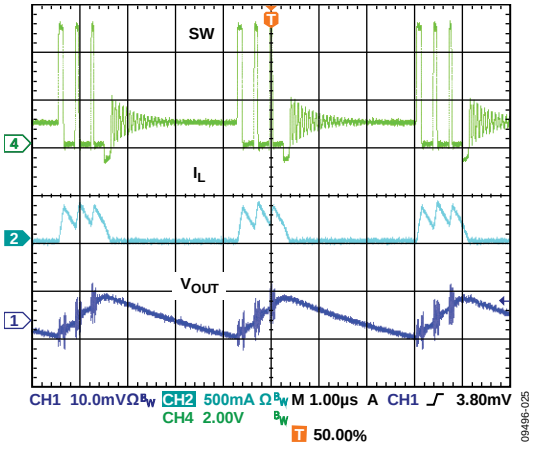

Figure 29. Typical Waveform, V_{OUT} = 1.8 V, PSM Mode, I_{OUT} = 10 mA

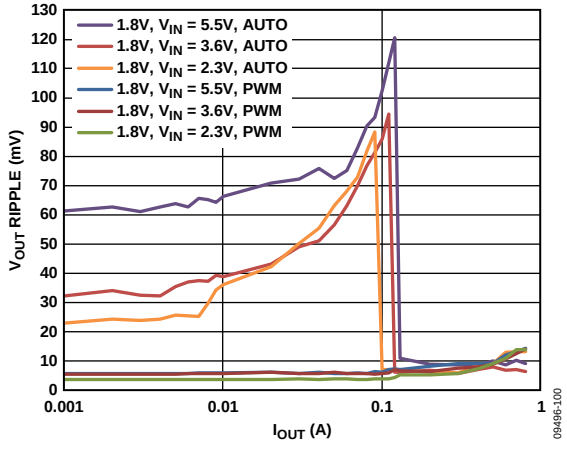

Figure 32. V_{OUT} Peak-to-Peak Ripple vs. Output Current, V_{OUT} = 1.8 V

THEORY OF OPERATION

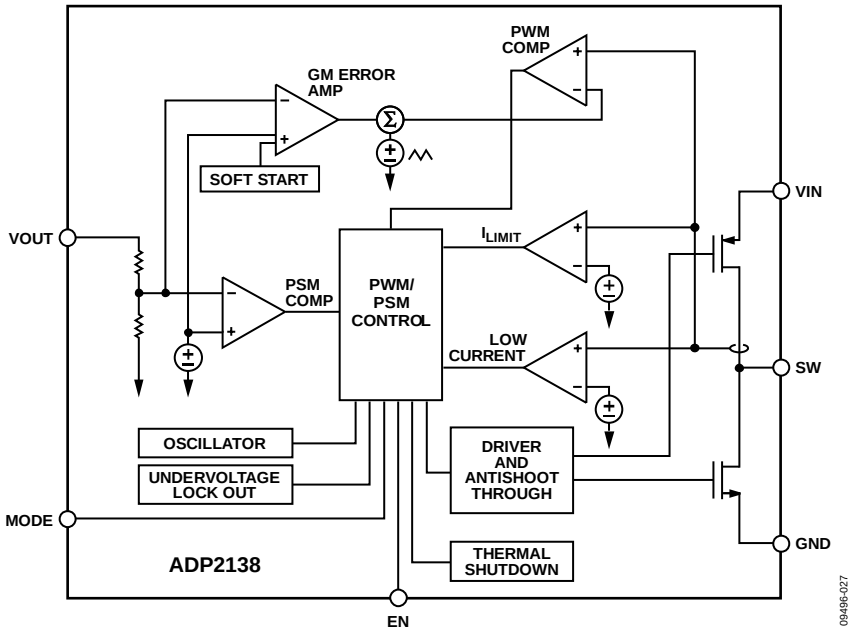

Figure 33. ADP2138 Functional Block Diagram

The ADP2138 and ADP2139 are step-down dc-to-dc converters that use a fixed frequency and high speed current-mode architecture. The high switching frequency and tiny 6-ball WLCSP package allow for a small step-down dc-to-dc converter solution.

The ADP2138/ADP2139 operate with an input voltage of 2.3 V to 5.5 V, and regulate an output voltage down to 0.8 V.

CONTROL SCHEME

The ADP2138/ADP2139 operate with a fixed frequency, current-mode PWM control architecture at medium to high loads for high efficiency, but shift to a power save mode control scheme at light loads to lower the regulation power losses. When operating in PWM mode, the duty cycle of the integrated switches is adjusted and regulates the output voltage. When operating in power save mode at light loads, the output voltage is controlled in a hysteretic manner, with higher V_{OUT} ripple. During part of this time, the converter is able to stop switching and enters an idle mode, which improves conversion efficiency. Each ADP2138/ADP2139 has a MODE pin, which determines the operation of the buck regulator in either PWM mode (when the MODE pin is set high) or power save mode (when the mode pin is set low).

PWM MODE

In PWM mode, the ADP2138/ADP2139 operate at a fixed frequency of 3 MHz, set by an internal oscillator. At the start of each oscillator cycle, the PFET switch is turned on, sending a positive voltage across the inductor. Current in the inductor increases until the current sense signal crosses the peak inductor current threshold that turns off the PFET switch and turns on the NFET synchronous rectifier. This sends a negative voltage across the inductor, causing the inductor current to decrease. The synchronous rectifier stays on for the rest of the cycle.

The ADP2138/ADP2139 regulate the output voltage by adjusting the peak inductor current threshold.

POWER SAVE MODE

The ADP2138/ADP2139 smoothly transition to the power save mode of operation when the load current decreases below the power save mode current threshold. When the ADP2138 and ADP2139 enter power save mode, an offset is induced in the PWM regulation level, which makes the output voltage rise. When the output voltage reaches a level approximately 1.5% above the PWM regulation level, PWM operation turns off. At this point, both power switches are off, and the ADP2138/ ADP2139 enter into idle mode. C_{OUT} discharges until V_{OUT} falls to the PWM regulation voltage, at which point the device drives the inductor to cause V_{OUT} to rise again to the upper threshold. This process is repeated for as long as the load current is below the power save mode current threshold.

Power Save Mode Current Threshold

The power save mode current threshold is set to 100 mA. The ADP2138/ADP2139 employ a scheme that enables this current to remain accurately controlled, independent of V_{IN} and V_{OUT} levels. This scheme also ensures that there is very little hysteresis between the power save mode current threshold for entry to and exit from the power save mode. The power save mode current threshold is optimized for excellent efficiency across all load currents.

ENABLE/SHUTDOWN

The ADP2138/ADP2139 start operating with soft start when the EN pin is toggled from logic low to logic high. Pulling the EN pin low forces the device into shutdown mode, reducing the shutdown current to 0.2 μA (typical).

SHORT-CIRCUIT PROTECTION

The ADP2138/ADP2139 include frequency fold back to prevent output current runaway on a hard short. When the voltage at the feedback pin falls below half the target output voltage, indicating the possibility of a hard short at the output, the switching frequency is reduced to half the internal oscillator frequency. The reduction in the switching frequency allows more time for the inductor to discharge, preventing a runaway of output current.

UNDERVOLTAGE LOCKOUT

To protect against battery discharge, undervoltage lockout (UVLO) circuitry is integrated on the ADP2138/ADP2139. If the input voltage drops below the 2.15 V UVLO threshold, the ADP2138/ADP2139 shut down, and both the power switch and the synchronous rectifier turn off. When the voltage rises above the UVLO threshold, the soft start period is initiated, and the part is enabled.

THERMAL PROTECTION

In the event that the ADP2138/ADP2139 junction temperature rises above 150°C, the thermal shutdown circuit turns off the converter. Extreme junction temperatures can be the result of high current operation, poor circuit board design, or high ambient temperature. A 20°C hysteresis is included so that when thermal shutdown occurs, the ADP2138/ADP2139 do not return to operation until the on-chip temperature drops below 130°C. When coming out of thermal shutdown, soft start is initiated.

SOFT START

The ADP2138/ADP2139 have an internal soft start function that ramps the output voltage in a controlled manner upon startup, thereby limiting the inrush current. This prevents possible input voltage drops when a battery or a high impedance power source is connected to the input of the converter.

After the EN pin is driven high, internal circuits begin to power up. Start-up time in the ADP2138/ADP2139 is the measure of when the output is in regulation after the EN pin is driven high. Start-up time consists of the power-up time and the soft start time.

CURRENT LIMIT

Each ADP2138/ADP2139 has protection circuitry to limit the amount of positive current flowing through the PFET switch and the synchronous rectifier. The positive current limit on the power switch limits the amount of current that can flow from the input to the output. The negative current limit prevents the inductor current from reversing direction and flowing out of the load.

100% DUTY OPERATION

With a drop in V_{IN} or with an increase in I_{LOAD}, the ADP2138/ADP2139 reach a limit where, even with the PFET switch on 100% of the time, V_{OUT} drops below the desired output voltage. At this limit, the ADP2138/ADP2139 smoothly transition to a mode where the PFET switch stays on 100% of the time. When the input conditions change again and the required duty cycle falls, the ADP2138/ADP2139 immediately restart PWM regulation without allowing overshoot on V_{OUT}.

DISCHARGE SWITCH

The ADP2139 has an integrated switched resistor (of typically 100 Ω) to discharge the output capacitor when the EN pin goes low or when the device enters undervoltage lockout or thermal shutdown. The time to discharge is typically 200 µs.

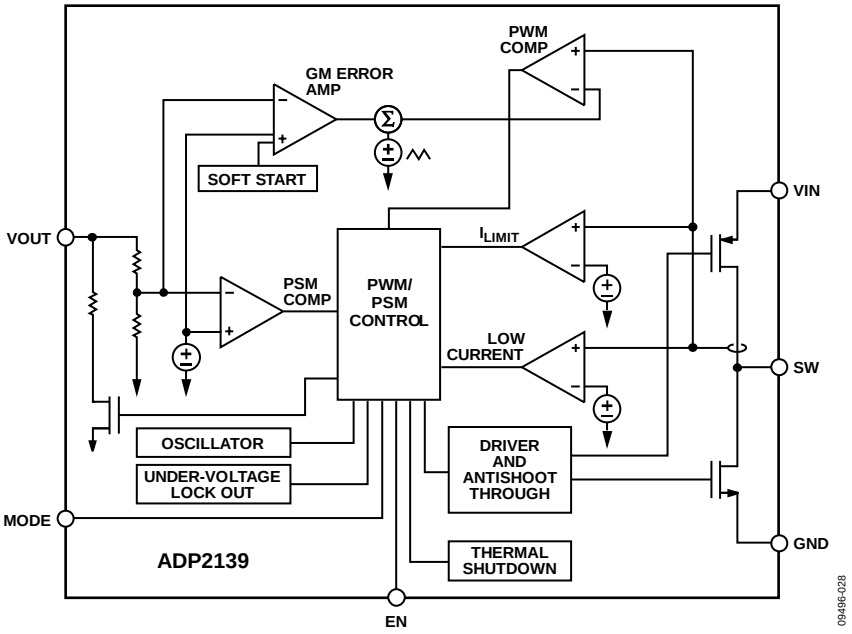

Figure 34. ADP2139 Functional Block Diagram

APPLICATIONS INFORMATION

ADIsimPower DESIGN TOOL

The ADP2138/ADP2139 is supported by ADIsimPower design tool set. ADIsimPower is a collection of tools that produce complete power designs optimized for a specific design goal. The tools enable the user to generate a full schematic, bill of materials, and calculate performance in minutes. ADIsimPower can optimize designs for cost, area, efficiency, and parts count while taking into consideration the operating conditions and limitations of the IC and all real external components. For more information about ADIsimPower design tools, refer to www.analog.com/ADIsimPower. The tool set is available from this website, and users can also request an unpopulated board through the tool.

EXTERNAL COMPONENT SELECTION

Trade-offs between performance parameters such as efficiency and transient response can be made by varying the choice of external components in the applications circuit, as shown in Figure 1.

Inductor

The high switching frequency of the ADP2138/ADP2139 allows for the selection of small chip inductors. For best performance, use inductor values between 0.7 µH and 3 µH. Recommended inductors are shown in Table 6.

The peak-to-peak inductor current ripple is calculated using the following equation:

$$I_{RIPPLE} = \frac{V_{OUT} \times (V_{IN} - V_{OUT})}{V_{IN} \times f_{SW} \times L}$$

where:
f_{SW} is the switching frequency.
L is the inductor value.

The minimum dc current rating of the inductor must be greater than the inductor peak current. The inductor peak current is calculated using the following equation:

$$I_{PEAK} = I_{LOAD(MAX)} + \frac{I_{RIPPLE}}{2}$$

Inductor conduction losses are caused by the flow of current through the inductor, which has an associated internal DCR. Larger sized inductors have smaller DCR, which may decrease inductor conduction losses. Inductor core losses are related to the magnetic permeability of the core material. Because the ADP2138/ADP2139 are high switching frequency dc-to-dc converters, shielded ferrite core material is recommended for its low core losses and low electromagnetic interference (EMI).

Table 6. Suggested 1.0 µH Inductors

Vendor	Model	Dimensions (mm)	I_{SAT} (mA)	DCR (mΩ)
Murata	LQM2MPN1R0NG0B	2.0 × 1.6 × 0.9	1400	85
	LQM18PN1R0	1.6 × 0.8 × 0.33	700	52
Taiyo Yuden	CBMF1608T1R0M	1.6 × 0.8 × 0.8	290	90
	EPL2014-102ML	2.0 × 2.0 × 1.4	900	59
Coilcraft TDK	GLFR1608T1R0M-LR	1.6 × 0.8 × 0.8	360	80
	0603LS-102	1.8 × 1.27 × 1.1	400	81
Coilcraft Toko	MDT2520-CN	2.5 × 2.0 × 1.2	1800	100

Output Capacitor

Higher output capacitor values reduce the output voltage ripple and improve load transient response. When choosing this value, it is also important to account for the loss of capacitance due to output voltage dc bias.

Ceramic capacitors are manufactured with a variety of dielectrics, each with different behavior over temperature and applied voltage. Capacitors must have a dielectric adequate to ensure the minimum capacitance over the necessary temperature range and dc bias conditions. X5R or X7R dielectrics with a voltage rating of 6.3 V or 10 V are recommended for best performance. Y5V and Z5U dielectrics are not recommended for use with any dc-to-dc converter because of their poor temperature and dc bias characteristics.

The worst-case capacitance accounting for capacitor variation over temperature, component tolerance, and voltage is calculated using the following equation:

$$C_{EFF} = C_{OUT} \times (1 - TEMPCO) \times (1 - TOL)$$

where:
C_{EFF} is the effective capacitance at the operating voltage.
$TEMPCO$ is the worst-case capacitor temperature coefficient.
TOL is the worst-case component tolerance.

In this example, the worst-case temperature coefficient (TEMPCO) over −40°C to +85°C is assumed to be 15% for an X5R dielectric. The tolerance of the capacitor (TOL) is assumed to be 10%, and C_{OUT} is 4.0466 µF at 1.8 V, as shown in Figure 35.

Substituting these values in the equation yields

$$C_{EFF} = 4.0466\ \mu F \times (1 - 0.15) \times (1 - 0.1) = 3.0956\ \mu F$$

To guarantee the performance of the ADP2138/ADP2139, it is imperative that the effects of dc bias, temperature, and tolerances on the behavior of the capacitors be evaluated for each application.

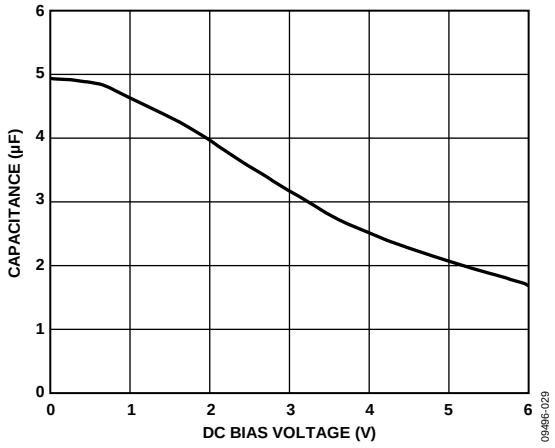

Figure 35. Typical Capacitor Performance

The peak-to-peak output voltage ripple for the selected output capacitor and inductor values is calculated using the following equation:

$$V_{RIPPLE} = \frac{V_{IN}}{(2\pi \times f_{SW}) \times 2 \times L \times C_{OUT}} = \frac{I_{RIPPLE}}{8 \times f_{SW} \times C_{OUT}}$$

Capacitors with lower equivalent series resistance (ESR) are preferred to guarantee low output voltage ripple, as shown in the following equation:

$$ESR_{COUT} \leq \frac{V_{RIPPLE}}{I_{RIPPLE}}$$

The effective capacitance needed for stability, which includes temperature and dc bias effects, is 3 µF.

Table 7. Suggested 4.7 µF Capacitors

Vendor	Type	Model	Case Size	Voltage Rating (V)
Murata	X5R	GRM188R60J475	0603	6.3
Taiyo Yuden	X5R	JMK107BJ475	0603	6.3
Coilcraft TDK	X5R	C1608X5R0J475	0603	6.3

Input Capacitor

Higher value input capacitors help to reduce the input voltage ripple and improve transient response. Maximum input capacitor current is calculated using the following equation:

$$I_{CIN} \geq I_{LOAD(MAX)} \sqrt{\frac{V_{OUT}(V_{IN} - V_{OUT})}{V_{IN}}}$$

To minimize supply noise, place the input capacitor as close to the VIN pin of the ADP2138/ADP2139 as possible. As with the output capacitor, a low ESR capacitor is recommended. The list of recommended capacitors is shown in Table 8.

Table 8. Suggested 4.7 µF Capacitors

Vendor	Type	Model	Case Size	Voltage Rating (V)
Murata	X5R	GRM188R60J475	0603	6.3
Taiyo Yuden	X5R	JMK107BJ475	0603	6.3
Coilcraft TDK	X5R	C1608X5R0J475	0603	6.3

THERMAL CONSIDERATIONS

Because of the high efficiency of the ADP2138/ADP2139, only a small amount of power is dissipated inside the ADP2138/ADP2139 package, which reduces thermal constraints.

However, in applications with maximum loads at high ambient temperature, low supply voltage, and high duty cycle, the heat dissipated in the package is great enough that it may cause the junction temperature of the die to exceed the maximum junction temperature of 125°C. If the junction temperature exceeds 150°C, the converter enters thermal shutdown. It recovers when the junction temperature falls below 130°C.

The junction temperature of the die is the sum of the ambient temperature of the environment and the temperature rise of the package due to power dissipation, as shown in the following equation:

$$T_J = T_A + T_R$$

where:
T_J is the junction temperature.
T_A is the ambient temperature.
T_R is the rise in temperature of the package due to power dissipation.

The rise in temperature of the package is directly proportional to the power dissipation in the package. The proportionality constant for this relationship is the thermal resistance from the junction of the die to the ambient temperature, as shown in the following equation:

$$T_R = \theta_{JA} \times P_D$$

where:
T_R is the rise in temperature of the package.
θ_{JA} is the thermal resistance from the junction of the die to the ambient temperature of the package.
P_D is the power dissipation in the package.

PCB LAYOUT GUIDELINES

Poor layout can affect ADP2138/ADP2139 performance, causing EMI and electromagnetic compatibility problems, ground bounce, and voltage losses. Poor layout can also affect regulation and stability. To implement a good layout, use the following rules:

- Place the inductor, input capacitor, and output capacitor close to the IC using short tracks. These components carry high switching frequencies, and large tracks act as antennas.
- Route the output voltage path away from the inductor and SW node to minimize noise and magnetic interference.
- Maximize the size of ground metal on the component side to help with thermal dissipation.
- Use a ground plane with several vias connecting to the component side ground to further reduce noise interference on sensitive circuit nodes.

EVALUATION BOARD

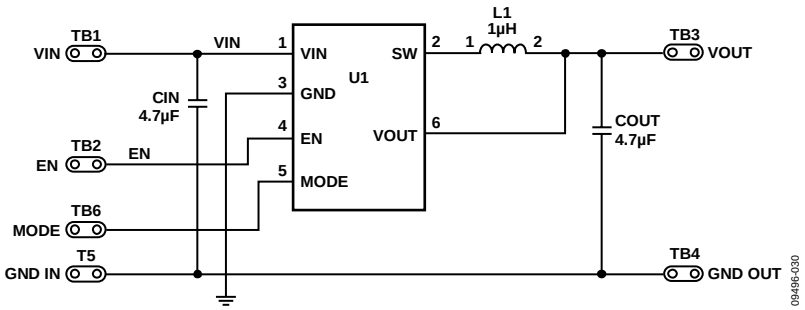

Figure 36. Evaluation Board Schematic

EVALUATION BOARD LAYOUT

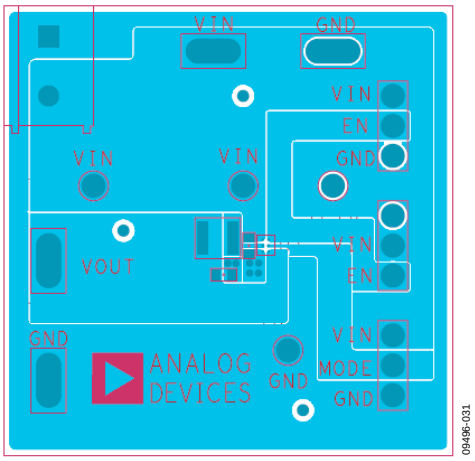

Figure 37. Top Layer

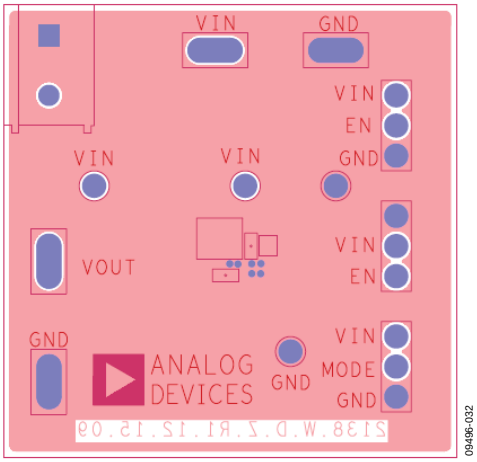

Figure 38. Bottom Layer

OUTLINE DIMENSIONS

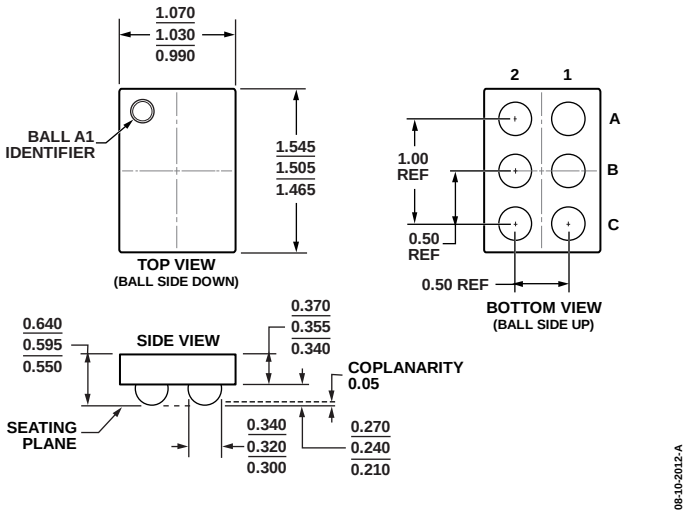

Figure 39. 6-Ball Wafer Level Chip Scale Package [WLCSP]
(CB-6-12)
Dimensions shown in millimeters

ORDERING GUIDE

Model[1]	Temperature Range	Output Voltage (V)	Package Description	Package Option	Branding
ADP2138ACBZ-0.8-R7	−40°C to +125°C	0.8	6-Ball Wafer Level Chip Scale Package [WLCSP]	CB-6-12	LJH
ADP2138ACBZ-1.0-R7	−40°C to +125°C	1.0	6-Ball Wafer Level Chip Scale Package [WLCSP]	CB-6-12	L88
ADP2138ACBZ-1.2-R7	−40°C to +125°C	1.2	6-Ball Wafer Level Chip Scale Package [WLCSP]	CB-6-12	L89
ADP2138ACBZ-1.5-R7	−40°C to +125°C	1.5	6-Ball Wafer Level Chip Scale Package [WLCSP]	CB-6-12	L8A
ADP2138ACBZ-1.8-R7	−40°C to +125°C	1.8	6-Ball Wafer Level Chip Scale Package [WLCSP]	CB-6-12	L8C
ADP2138ACBZ-2.5-R7	−40°C to +125°C	2.5	6-Ball Wafer Level Chip Scale Package [WLCSP]	CB-6-12	L93
ADP2138ACBZ-2.8-R7	−40°C to +125°C	2.8	6-Ball Wafer Level Chip Scale Package [WLCSP]	CB-6-12	LDH
ADP2138ACBZ-3.0-R7	−40°C to +125°C	3.0	6-Ball Wafer Level Chip Scale Package [WLCSP]	CB-6-12	LDJ
ADP2138ACBZ-3.3-R7	−40°C to +125°C	3.3	6-Ball Wafer Level Chip Scale Package [WLCSP]	CB-6-12	LDP
ADP2139ACBZ-0.8-R7	−40°C to +125°C	0.8	6-Ball Wafer Level Chip Scale Package [WLCSP]	CB-6-12	LJJ
ADP2139ACBZ-1.0-R7	−40°C to +125°C	1.0	6-Ball Wafer Level Chip Scale Package [WLCSP]	CB-6-12	LHN
ADP2139ACBZ-1.2-R7	−40°C to +125°C	1.2	6-Ball Wafer Level Chip Scale Package [WLCSP]	CB-6-12	LHP
ADP2139ACBZ-1.5-R7	−40°C to +125°C	1.5	6-Ball Wafer Level Chip Scale Package [WLCSP]	CB-6-12	LHQ
ADP2139ACBZ-1.8-R7	−40°C to +125°C	1.8	6-Ball Wafer Level Chip Scale Package [WLCSP]	CB-6-12	LHR
ADP2139ACBZ-2.5-R7	−40°C to +125°C	2.5	6-Ball Wafer Level Chip Scale Package [WLCSP]	CB-6-12	LHS
ADP2139ACBZ-2.8-R7	−40°C to +125°C	2.8	6-Ball Wafer Level Chip Scale Package [WLCSP]	CB-6-12	LHT
ADP2139ACBZ-3.0-R7	−40°C to +125°C	3.0	6-Ball Wafer Level Chip Scale Package [WLCSP]	CB-6-12	LHU
ADP2139ACBZ-3.3-R7	−40°C to +125°C	3.3	6-Ball Wafer Level Chip Scale Package [WLCSP]	CB-6-12	LHV
ADP2138CB-0.8EVALZ			Evaluation Board		
ADP2138CB-1.0EVALZ			Evaluation Board		
ADP2138CB-1.2EVALZ			Evaluation Board		
ADP2138CB-1.5EVALZ			Evaluation Board		
ADP2138CB-1.8EVALZ			Evaluation Board		
ADP2138CB-2.5EVALZ			Evaluation Board		
ADP2138CB-2.8EVALZ			Evaluation Board		
ADP2138CB-3.0EVALZ			Evaluation Board		
ADP2138CB-3.3EVALZ			Evaluation Board		
ADP2139CB-0.8EVALZ			Evaluation Board		
ADP2139CB-1.0EVALZ			Evaluation Board		
ADP2139CB-1.2EVALZ			Evaluation Board		
ADP2139CB-1.5EVALZ			Evaluation Board		
ADP2139CB-1.8EVALZ			Evaluation Board		
ADP2139CB-2.5EVALZ			Evaluation Board		
ADP2139CB-2.8EVALZ			Evaluation Board		
ADP2139CB-3.0EVALZ			Evaluation Board		
ADP2139CB-3.3EVALZ			Evaluation Board		

[1] Z = RoHS Compliant Part.

NOTES

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