

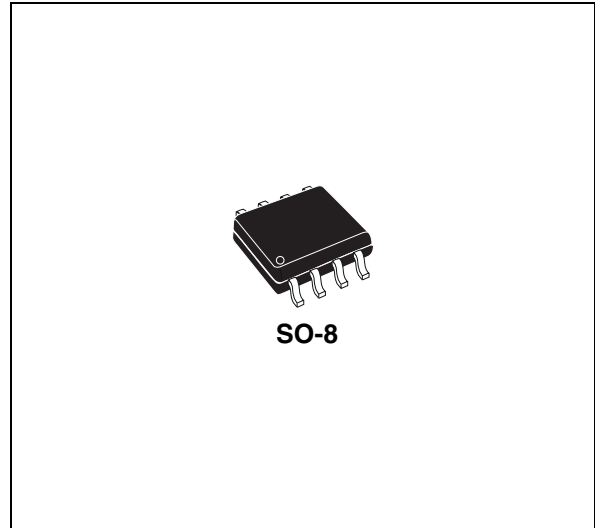
High voltage high-side driver

Features

- High voltage rail up to 450 V
- dV/dt immunity ± 50 V/nsec in full temperature range
- Driver current capability:
500 mA source,
500 mA sink
- Switching times 100 ns rise/fall with 2.5 nF load
- CMOS/TTL Schmitt trigger inputs with hysteresis and pull down
- Under voltage lock out
- Clamping on V_{CC}
- Non inverting input
- Reset circuitry
- SO8 package

Description

The L9857 is an high voltage device, manufactured with the BCD "off-line" technology.



It has the capability of driving N channel PowerMOS transistors. The upper (floating) section is enabled to work with voltage rail up to 450 V. The logic inputs are CMOS/TTL compatible for ease of interfacing with controlling devices..

Table 1. Device summary

Order code	Op. temp range, °C	Package	Packing
L9857-TR	-40 to +125	SO-8	Tape and reel
L9857-TR-LF	-40 to +125	SO-8	Tape and reel

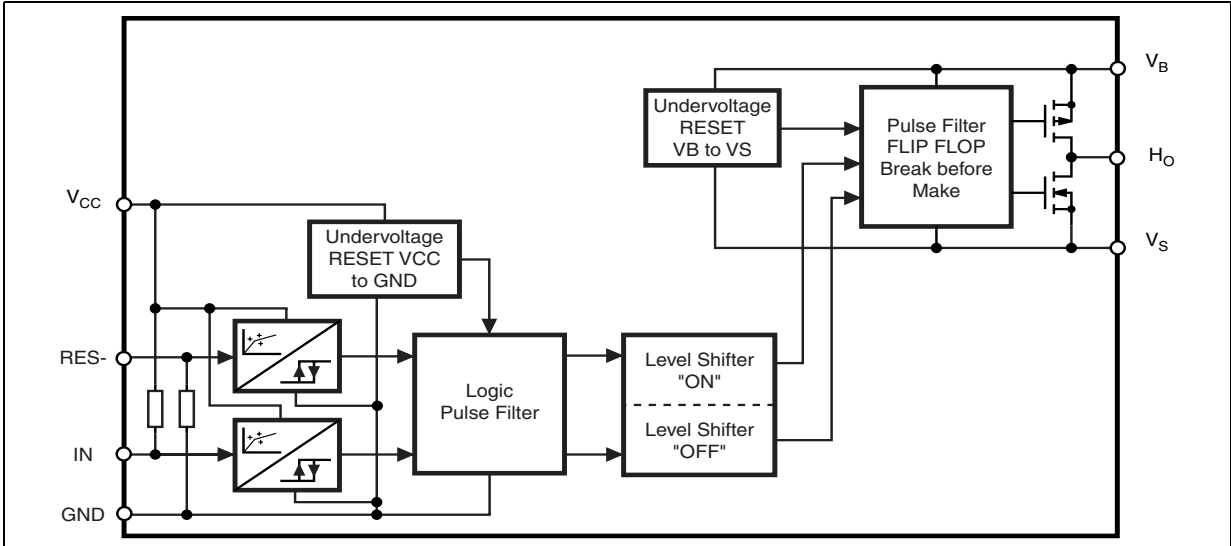
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1 Block diagram and pin description

1.1 Block diagram

Figure 1. Block diagram



1.2 Pin description

Figure 2. Pin connection (top view)

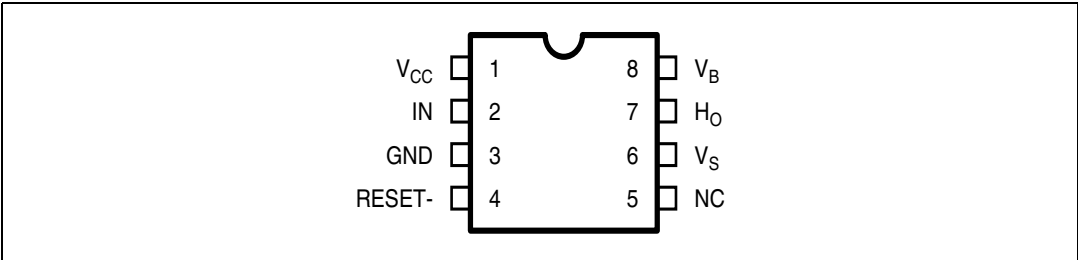


Table 2. Pin function

Pin #	Pin name	Description
1	V _{CC}	Driver supply, typically 17V
2	IN	Driver control signal input (positive logic)
3	GND	Ground
4	RESET-	Driver enable signal input (negative logic)
5	NC	No connection (no bondwire)
6	V _S	MOSFET source connection
7	H _O	MOSFET gate connection
8	V _B	Driver output stage supply

2 Electrical specifications

2.1 Thermal data

Table 3. Thermal data

Symbol	Parameter	Value	Unit
$R_{th(j-amb)}$	Thermal resistance junction-to-ambient	Max. 150	°C/W

2.2 Absolute maximum ratings

Absolute maximum ratings indicate sustained limits beyond which damage to the device may occur. All voltage parameters are absolute voltages referenced to GND, all currents are defined positive into any lead. This is a stress only rating and operation of the device at these or any conditions exceeding those indicated in the operational sections of this specifications is not implied.

Table 4. Absolute maximum ratings

Parameter		Value		Units
Symbol	Definition	Min.	Max.	
V_{BS}	High side floating supply voltage	-0.3	20	V
V_B	High side driver output stage voltage	-0.3	300	V
V_S	High side floating supply offset voltage	$V_B - 20$	300	V
V_{HO}	Output voltage gate connection	$V_S - 0.3$	$V_B + 0.3$	V
V_{CC}	Supply voltage	-0.3	20	V
V_{IN}	Input voltage	-0.3	$V_{CC} + 0.3$	V
I_{IN}	Input injection current. Full function, no latch-up; (guaranteed by design). Test at 10 V and 17 V on eng. samples.	-	+1	mA
V_{RES}	Reset input voltage	-0.3	$V_{CC} + 0.3$	V
V_{esd}	Electrostatic discharge voltage (human body model)	2k	-	V
V_{CDM}	Charge device model CDM, EOS/ESD ass. std 5.3. number of discharges per pin: 6	500	-	V
dV/dt	Allowable offset voltage slew rate	-50	50	V/nsec
T_j	Junction temperature	-55	150	°C
T_{stg}	Storage temperature	-55	150	
T_L	Lead temperature (soldering, 10 seconds) 3 times Bosch soldering profil acc. to Bosch soldering conditions, gen. spec.	-	300	

2.3 Recommended operating conditions

For proper operations the device should be used within the recommended conditions.

Table 5. Recommended operating conditions

Parameter		Value		Units
Symbol	Definition	Min.	Max.	
V_B	High side driver output stage voltage -5 V transient 0.1 μ s	V_S+10 ⁽¹⁾	V_S+18	V
V_S	High side floating supply offset voltage - 20 V transient 0.1 μ s	-5	300	V
V_{HO}	Output voltage gate connection	V_S	V_B	V
V_{CC}	Supply voltage	10	18	V
V_{IN}	Input voltage	0	V_{CC}	V
V_{RES}	Reset input voltage	0	V_{CC}	V
F_S	Switching frequency	-	200	kHz
T_{amb}	Ambient temperature	-40	125	°C

1. Reset-Logic functional for $V_B-V_S=2V$, independent from V_{CC} -level

2.4 Electrical characteristics

Unless otherwise specified, $V_{CC} = 15$ V, $V_{BS} = 15$ V, $V_S = 0$ V, $I_N = 0$ V, $R_{ES} = 5$ V, load $R = 50$ Ω , $C = 2.5$ nF. Unless otherwise noted, these specifications apply for an operating junction temperature range of -40 °C $\leq T_j \leq 125$ °C

Table 6. Electrical characteristics

Symbol	Parameter	Test condition	Min.	Typ.	Max.	Unit
V_{CC} supply						
V_{CCUV}	V_{CC} supply undervoltage	V_{CC} rising from 0 V V_{CC} dropping from 10 V	7.2	-	9.6	V
$V_{CCUVHYS}$	V_{CC} supply undervoltage lockout hysteresis	-	0.02	0.2	0.4	V
t_{dUVCC}	Undervoltage lockout response time	V_{CC} steps either from 10 V to 6 V or from 6 V to 10 V	0.5	-	20	μ s
I_{QCC}	V_{CC} supply current	-	-	-	400	μ A
V_{BS} supply						
V_{BSUV}	V_{BS} supply undervoltage	V_{BS} rising from 0 V V_{BS} dropping from 10 V	7.2	-	9.6	V
t_{dUVBS}	Undervoltage lockout response time	V_{BS} steps either from 10 V to 6 V or from 6 V to 10 V	0.5	-	20	μ s

Table 6. Electrical characteristics (continued)

Symbol	Parameter	Test condition	Min.	Typ.	Max.	Unit
$V_{BSUVHYS}$	V_{BS} supply undervoltage lockout hysteresis	-	0.02	0.2	0.4	V
I_{QBS1}	V_{BS} supply current	static mode, $V_{BS} = 10\text{ V}$, $I_N = 0\text{ V}$ or 5 V	-	-	100	μA
I_{QBS2}		static mode, $V_{BS} = 18\text{ V}$, $I_N = 0\text{ V}$ or V_{CC}	-	-	200	μA
ΔV_{BS}	V_{BS} drop due to output turn-on	$V_{BS} = 17\text{ V}$, $C_{BS} = 1\text{ }\mu\text{F}$, $t_{dIG-IN} = 3\text{ }\mu\text{s}$, $t_{TEST} = 100\text{ }\mu\text{s}$	-	-	210	mV
Gate driver characteristics						
I_{PKSo1}	Peak output source current	$V_{BS} = 10\text{ V}$, $T_j = 25\text{ }^\circ\text{C}$ $PW \leq 10\text{ }\mu\text{s}$	120	250	-	mA
I_{PKSo2}		$V_{BS} = 10\text{ V}$ $PW \leq 10\text{ }\mu\text{s}$	70	150	-	
I_{PKSo3}		$V_{BS} = 17\text{ V}$, $T_j = 25\text{ }^\circ\text{C}$ $PW \leq 10\text{ }\mu\text{s}$	250	500	-	
I_{PKSo4}		$V_{BS} = 17\text{ V}$, $PW \leq 10\text{ }\mu\text{s}$	150	300	-	
$I_{HOH,off}$	HOH off-state leakage current	Guaranteed by design	-	-	1	μA
t_{r1}	Output rise time	$V_{BS} = 10\text{ V}$, $T_j = 25\text{ }^\circ\text{C}$	-	0.2	0.4	μs
t_{r2}		$V_{BS} = 10\text{ V}$	-	0.3	0.5	
t_{r3}		$V_{BS} = 17\text{ V}$, $T_j = 25\text{ }^\circ\text{C}$	-	0.1	0.2	
t_{r4}		$V_{BS} = 17\text{ V}$	-	0.15	0.3	
I_{PKSi1}	Peak output sink current	$I_N = V_{CC}$, $T_j = 25\text{ }^\circ\text{C}$ $V_{BS} = 10\text{ V}$, $PW < 10\text{ }\mu\text{s}$	120	250	-	mA
I_{PKSi2}		$I_N = V_{CC}$, $V_{BS} = 10\text{ V}$, $PW < 10\text{ }\mu\text{s}$	70	150	-	
I_{PKSi3}		$I_N = V_{CC}$, $T_j = 25\text{ }^\circ\text{C}$ $V_{BS} = 17\text{ V}$, $PW < 10\text{ }\mu\text{s}$	250	500	-	
I_{PKSi4}		$I_N = V_{CC}$, $V_{BS} = 17\text{ V}$, $PW < 10\text{ }\mu\text{s}$	150	300	-	
t_{f1}	Output fall time	$V_{BS} = 10\text{ V}$, $T_j = 25\text{ }^\circ\text{C}$	-	0.2	0.4	μs
t_{f2}		$V_{BS} = 10\text{ V}$	-	0.3	0.5	
t_{f3}		$V_{BS} = 17\text{ V}$, $T_j = 25\text{ }^\circ\text{C}$	-	0.1	0.2	
t_{f4}		$V_{BS} = 17\text{ V}$	-	0.15	0.3	
t_{plh}	Input-to-output turn-on propagation delay (50 % input level to 10 % output level)	-	-	0.1	0.3	μs

Table 6. Electrical characteristics (continued)

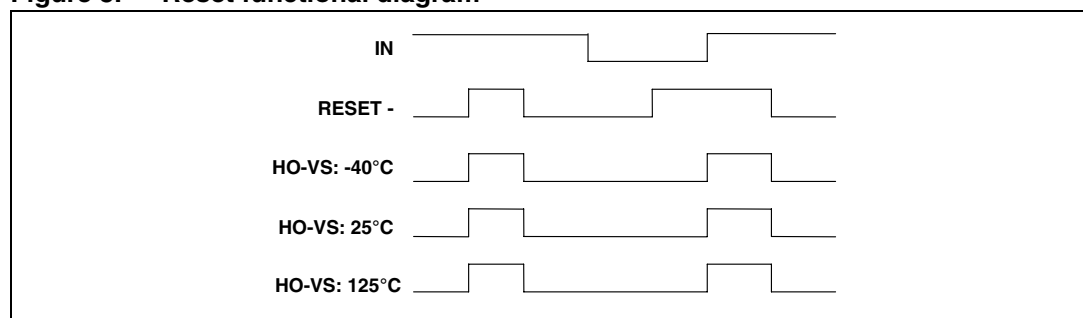
Symbol	Parameter	Test condition	Min.	Typ.	Max.	Unit
t _{phl}	Input-to-output turn-off propogation delay (50 % input level to 90% output level)	-	-	0.1	0.2	μs
t _{phl_res}	RES-to-output turn-off propogation delay (50% input level to 90% output levels)	-	-	0.1	0.3	
t _{plh_res}	RES-to-output turn-on propogation delay (50% input level to 10% output levels)	-	-	0.1	0.8	
Input characteristics						
V _{INH}	High logic level input threshold	-	9.5	-	-	V
V _{INL}	Low logic level input threshold	-	-	-	6	
R _{IN}	High logic level input resistance (Pull-down resistor)	-	60	-	300	kΩ
I _{IN}	Low logic level input current	V _{IN} = 0	-	-	5	μA
V _{H_RES}	High logic level RES input threshold	Reset signal comes from a 5 V system!	3.5	-	-	V
V _{L_RES}	Low Logic Level RES input threshold	R eset signal comes from a 5V system!	-	-	1.4	
R _{RES}	High logic level RES input resistance (Pull-down resistor)	Reset signal comes from a 5 V system with pull-up resistor 3.8 kΩ to 5 V. ⁽¹⁾	60	-	300	kΩ
I _{RES}	Low logic level input current	V _{RES} = 0	-	-	5	μA

1. 4 HS-driver reset- inputs and other IC with their input pull-down resistors are connected in parallel with the RESET wire. The enable input RES- is an active low input, that means a logic low turns the external Power MOSFET off. The input circuitry has to make sure, that the MOSFET is off, when the pin is open or floating. In the application the RES- pin is tied to a bipolar open collector transistor or MOSFET open drain transistor with pull-up resistor 3.8K to +5V together with other RES- inputs of other IC.

2.5 Reset functional diagram

The diagram is guaranteed for the following condition.

$V_{CC} = 10\text{ V}$; $V_{BS} = 10\text{ V}$ @ $-40\text{ }^{\circ}\text{C}$, $V_{CC} = 17\text{ V}$; $V_{BS} = 17\text{ V}$ @ $+25\text{ }^{\circ}\text{C}$ and $125\text{ }^{\circ}\text{C}$

Figure 3. Reset functional diagram

3 Timing diagrams

Figure 4. Input/output timing diagram

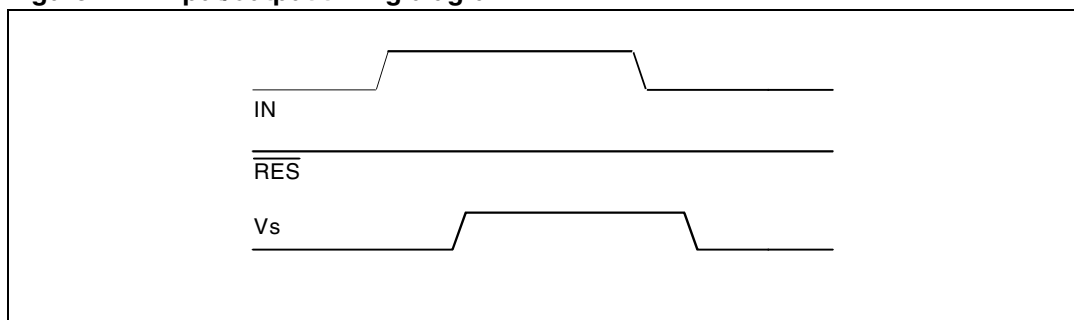
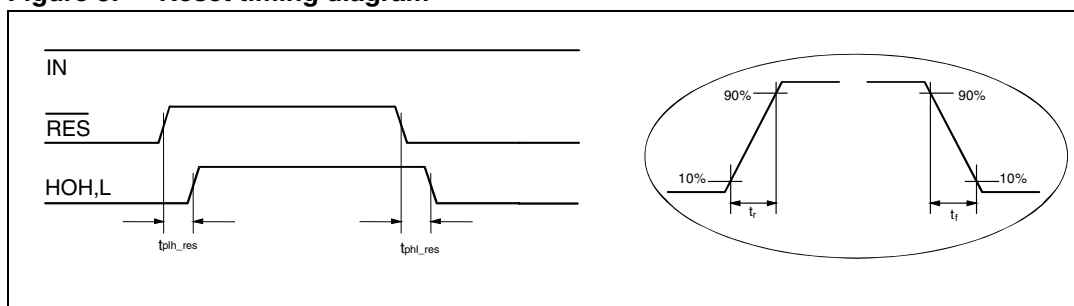


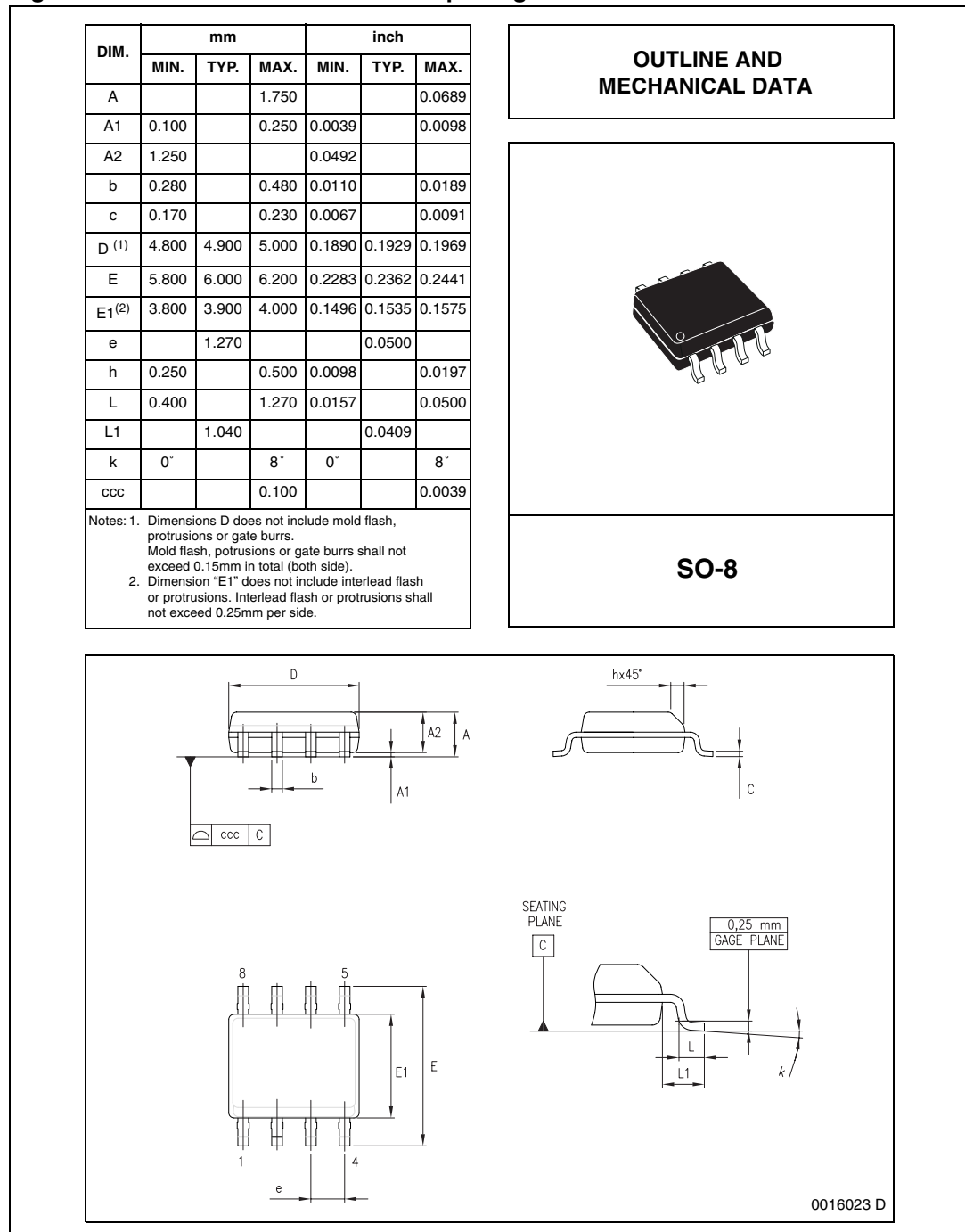
Figure 5. Reset timing diagram



4 Package information

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Figure 6. SO-8 mechanical data and package dimensions



5 Revision history

Table 7. Document revision history

Date	Revision	Changes
20-Nov-2006	1	Initial release.
07-Oct-2009	2	Updated Table 1: Device summary .

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