

# DATA SHEET

**74LVT32**

**3.3 V Quad 2-input OR gate**

Product data  
Supersedes data of 1996 Aug 28

2002 Sep 06

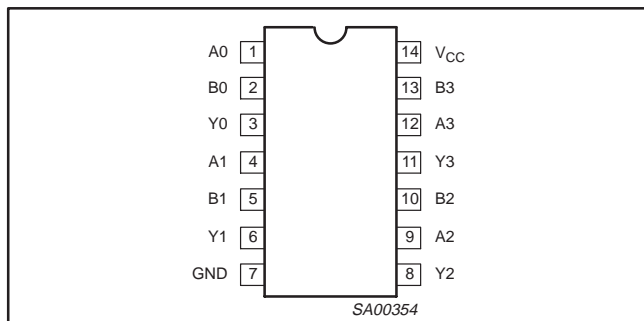
# 3.3 V Quad 2-input OR gate

# 74LVT32

### QUICK REFERENCE DATA

SYMBOL	PARAMETER	CONDITIONS $T_{amb} = 25\text{ }^{\circ}\text{C};$ $GND = 0\text{ V}$	TYPICAL	UNIT
$t_{PLH}$ $t_{PHL}$	Propagation delay An, Bn to Yn	$C_L = 50\text{ pF};$ $V_{CC} = 3.3\text{ V}$	2.6 3.2	ns
$C_{IN}$	Input capacitance	$V_I = 0\text{ V or }3.0\text{ V}$	3	pF
$I_{CCL}$	Total supply current	Outputs Low; $V_{CC} = 3.6\text{ V}$	1	mA

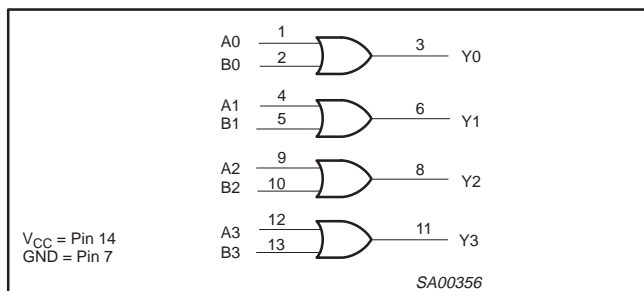
### PIN CONFIGURATION



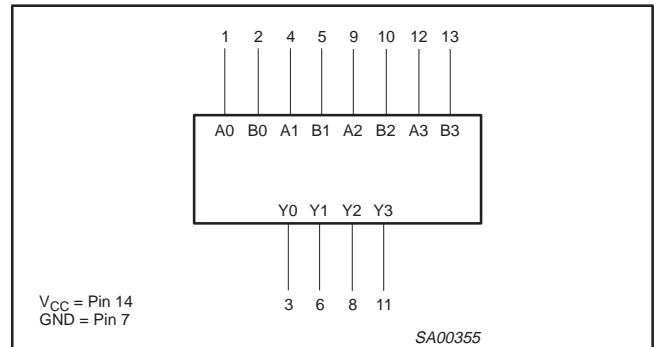
### PIN DESCRIPTION

PIN NUMBER	SYMBOL	NAME AND FUNCTION
1, 2, 4, 5, 9, 10, 12, 13	An, Bn	Data inputs
3, 6, 8, 11	Yn	Data outputs
7	GND	Ground (0 V)
14	$V_{CC}$	Positive supply voltage

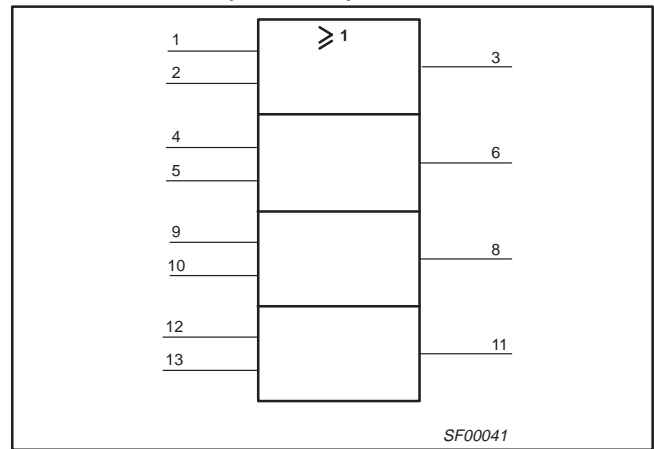
### LOGIC DIAGRAM



### LOGIC SYMBOL



### LOGIC SYMBOL (IEEE/IEC)



### FUNCTION TABLE

INPUTS		OUTPUT
Dna	Dnb	Qn
L	L	L
L	H	H
H	L	H
H	H	H

#### NOTES:

- H = High voltage level
- L = Low voltage level

### ORDERING INFORMATION

PACKAGES	TEMPERATURE RANGE	OUTSIDE NORTH AMERICA	NORTH AMERICA	DWG NUMBER
14-Pin Plastic SO	-40 °C to +85 °C	74LVT32D	74LVT32D	SOT108-1
14-Pin Plastic SSOP	-40 °C to +85 °C	74LVT32DB	74LVT32DB	SOT337-1
14-Pin Plastic TSSOP	-40 °C to +85 °C	74LVT32PW	74LVT32PWDH	SOT402-1

## 3.3 V Quad 2-input OR gate

74LVT32

**ABSOLUTE MAXIMUM RATINGS<sup>1, 2</sup>**

SYMBOL	PARAMETER	CONDITIONS	RATING	UNIT
V <sub>CC</sub>	DC supply voltage		-0.5 to +4.6	V
I <sub>IK</sub>	DC input diode current	V <sub>I</sub> < 0	-50	mA
V <sub>I</sub>	DC input voltage <sup>3</sup>		-0.5 to +7.0	V
I <sub>OK</sub>	DC output diode current	V <sub>O</sub> < 0	-50	mA
V <sub>OUT</sub>	DC output voltage <sup>3</sup>	Output in Off or High state	-0.5 to +7.0	V
I <sub>OUT</sub>	DC output current	Output in High state	-32	mA
		Output in Low state	64	
T <sub>stg</sub>	Storage temperature range		-65 to 150	°C

**NOTES:**

- Stresses beyond those listed may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
- The performance capability of a high-performance integrated circuit in conjunction with its thermal environment can create junction temperatures which are detrimental to reliability. The maximum junction temperature of this integrated circuit should not exceed 150°C.
- The input and output negative voltage ratings may be exceeded if the input and output clamp current ratings are observed.

**RECOMMENDED OPERATING CONDITIONS**

SYMBOL	PARAMETER	LIMITS		UNIT
		MIN	MAX	
V <sub>CC</sub>	DC supply voltage	2.7	3.6	V
V <sub>I</sub>	Input voltage	0	5.5	V
V <sub>IH</sub>	High-level input voltage	2.0		V
V <sub>IL</sub>	Low-level Input voltage		0.8	V
I <sub>OH</sub>	High-level output current		-20	mA
I <sub>OL</sub>	Low-level output current		32	mA
Δt/Δv	Input transition rise or fall rate; Outputs enabled		10	ns/V
T <sub>amb</sub>	Operating free-air temperature range	-40	+85	°C

### 3.3 V Quad 2-input OR gate

74LVT32

#### DC ELECTRICAL CHARACTERISTICS

Over recommended operating conditions  
 Voltages are referenced to GND (ground = 0 V)

SYMBOL	PARAMETER	TEST CONDITIONS	LIMITS			UNIT
			Temp = -40°C to +85°C			
			MIN	TYP <sup>1</sup>	MAX	
$V_{IK}$	Input clamp voltage	$V_{CC} = 2.7\text{ V}; I_{IK} = -18\text{ mA}$			-1.2	V
$V_{OH}$	High-level output voltage	$V_{CC} = 2.7\text{ to }3.6\text{ V}; I_{OH} = -100\text{ }\mu\text{A}$	$V_{CC}-0.2$			V
		$V_{CC} = 2.7\text{ V}; I_{OH} = -6\text{ mA}$	2.4			
		$V_{CC} = 3.0\text{ V}; I_{OH} = -20\text{ mA}$	2.0			
$V_{OL}$	Low-level output voltage	$V_{CC} = 2.7\text{ V}; I_{OL} = 100\text{ }\mu\text{A}$	0.2			V
		$V_{CC} = 2.7\text{ V}; I_{OL} = 24\text{ mA}$	0.5			
		$V_{CC} = 3.0\text{ V}; I_{OL} = 32\text{ mA}$	0.5			
$I_I$	Input leakage current	$V_{CC} = 0\text{ or }3.6\text{ V}; V_I = 5.5\text{ V}$	10			$\mu\text{A}$
		$V_{CC} = 3.6\text{ V}; V_I = V_{CC}\text{ or GND}$	$\pm 1$			
$I_{OFF}$	Output off current	$V_{CC} = 0\text{ V}; V_I\text{ or }V_O = 0\text{ to }4.5\text{ V}$	$\pm 100$			$\mu\text{A}$
$I_{CCH}$	Quiescent supply current	$V_{CC} = 3.6\text{ V};$ Outputs High, $V_I = \text{GND or }V_{CC}, I_O = 0$	0.02			mA
$I_{CCL}$		$V_{CC} = 3.6\text{ V};$ Outputs Low, $V_I = \text{GND or }V_{CC}, I_O = 0$	1	2		
$\Delta I_{CC}$	Additional supply current per input pin <sup>2</sup>	$V_{CC} = 3\text{ V to }3.6\text{ V};$ One input at $V_{CC}-0.6\text{ V},$ Other inputs at $V_{CC}\text{ or GND}$	0.2			$\mu\text{A}$
$C_I$	Input capacitance	$V_I = 3\text{ V or }0$	3			pF

**NOTES:**

1. All typical values are at  $V_{CC} = 3.3\text{ V}$  and  $T_{amb} = 25\text{ }^\circ\text{C}$ .
2. This is the increase in supply current for each input at the specified voltage level other than  $V_{CC}$  or GND.

#### AC CHARACTERISTICS

$\text{GND} = 0\text{ V}; t_R = t_F = 2.5\text{ ns}; C_L = 50\text{ pF}, R_L = 500\text{ }\Omega; T_{amb} = -40\text{ }^\circ\text{C to }+85\text{ }^\circ\text{C}.$

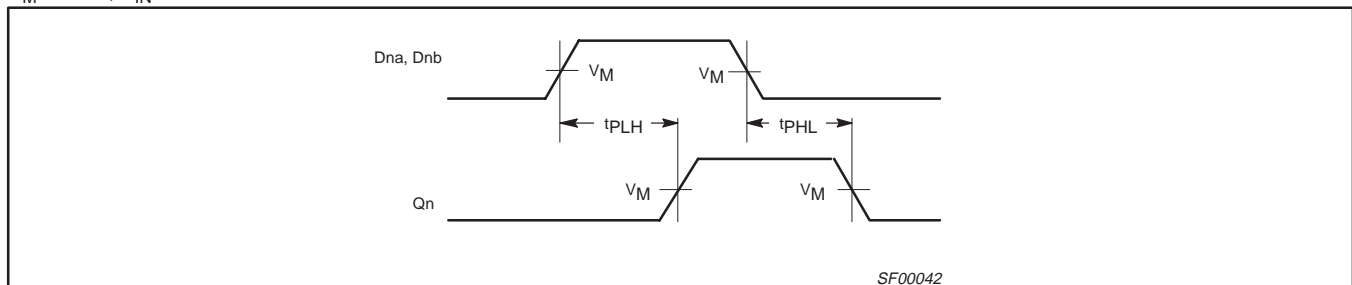
SYMBOL	PARAMETER	WAVEFORM	LIMITS				UNIT
			$V_{CC} = 3.3\text{ V} \pm 0.3\text{ V}$			$V_{CC} = 2.7\text{ V}$	
			MIN	TYP <sup>1</sup>	MAX	MAX	
$t_{PLH}$ $t_{PHL}$	Propagation delay An, Bn to Yn	1	1.0 1.0	2.6 3.2	3.8 4.6	4.5 4.9	ns

**NOTE:**

1. All typical values are at  $V_{CC} = 3.3\text{ V}$  and  $T_{amb} = 25\text{ }^\circ\text{C}$ .

#### AC WAVEFORMS

$V_M = 1.5\text{ V}, V_{IN} = \text{GND to }2.7\text{ V}$

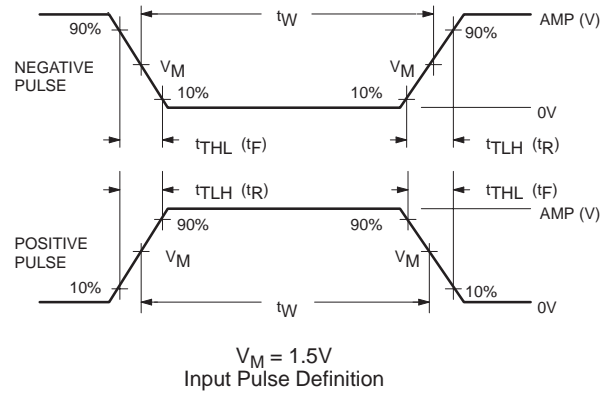
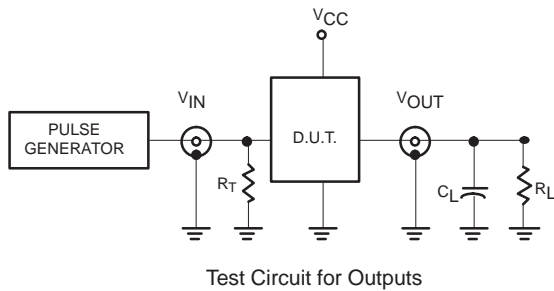


Waveform 1. Propagation delay for inverting outputs

### 3.3 V Quad 2-input OR gate

### 74LVT32

#### TEST CIRCUIT AND WAVEFORMS



#### DEFINITIONS

- $R_L$  = Load resistor; see AC CHARACTERISTICS for value.
- $C_L$  = Load capacitance includes jig and probe capacitance; see AC CHARACTERISTICS for value.
- $R_T$  = Termination resistance should be equal to  $Z_{OUT}$  of pulse generators.

FAMILY	INPUT PULSE REQUIREMENTS				
	Amplitude	Rep. Rate	$t_w$	$t_r$	$t_f$
74LVT	2.7V	$\leq 10MHz$	500ns	$\leq 2.5ns$	$\leq 2.5ns$

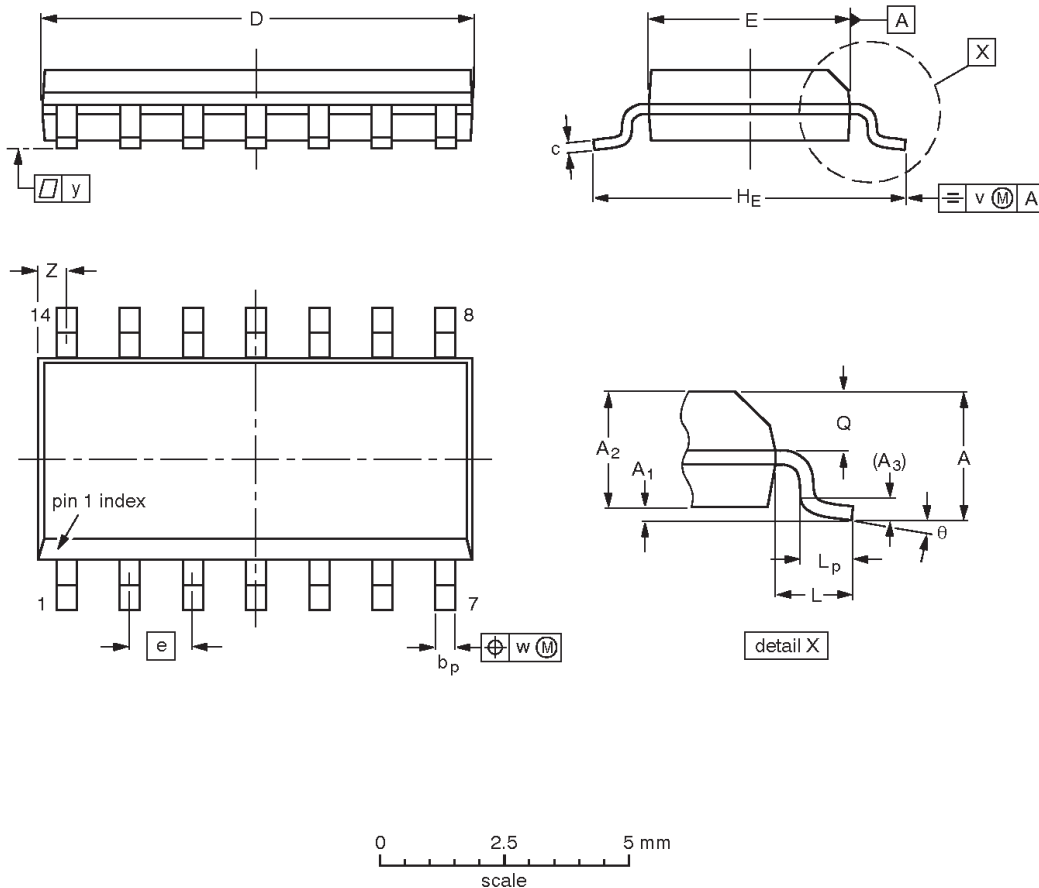
SV00022

# 3.3 V Quad 2-input OR gate

# 74LVT32

**SO14: plastic small outline package; 14 leads; body width 3.9 mm**

**SOT108-1**



**DIMENSIONS (inch dimensions are derived from the original mm dimensions)**

UNIT	A max.	A <sub>1</sub>	A <sub>2</sub>	A <sub>3</sub>	b <sub>p</sub>	c	D <sup>(1)</sup>	E <sup>(1)</sup>	e	H <sub>E</sub>	L	L <sub>p</sub>	Q	v	w	y	z <sup>(1)</sup>	θ
mm	1.75	0.25 0.10	1.45 1.25	0.25	0.49 0.36	0.25 0.19	8.75 8.55	4.0 3.8	1.27	6.2 5.8	1.05	1.0 0.4	0.7 0.6	0.25	0.25	0.1	0.7 0.3	8° 0°
inches	0.069	0.010 0.004	0.057 0.049	0.01	0.019 0.014	0.0100 0.0075	0.35 0.34	0.16 0.15	0.050	0.244 0.228	0.041	0.039 0.016	0.028 0.024	0.01	0.01	0.004	0.028 0.012	

**Note**

1. Plastic or metal protrusions of 0.15 mm maximum per side are not included.

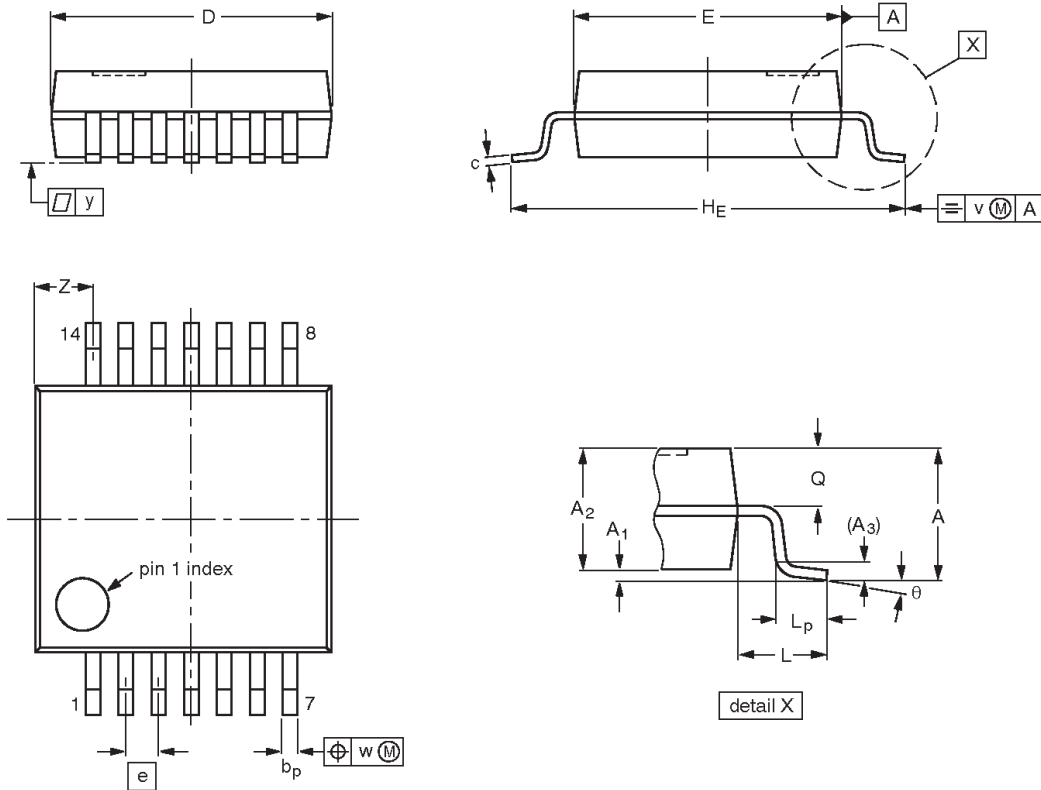
OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	EIAJ			
SOT108-1	076E06	MS-012				97-05-22 99-12-27

# 3.3 V Quad 2-input OR gate

# 74LVT32

**SSOP14:** plastic shrink small outline package; 14 leads; body width 5.3 mm

**SOT337-1**



**DIMENSIONS (mm are the original dimensions)**

UNIT	A max.	A <sub>1</sub>	A <sub>2</sub>	A <sub>3</sub>	b <sub>p</sub>	c	D <sup>(1)</sup>	E <sup>(1)</sup>	e	H <sub>E</sub>	L	L <sub>p</sub>	Q	v	w	y	Z <sup>(1)</sup>	θ
mm	2.0	0.21 0.05	1.80 1.65	0.25	0.38 0.25	0.20 0.09	6.4 6.0	5.4 5.2	0.65	7.9 7.6	1.25	1.03 0.63	0.9 0.7	0.2	0.13	0.1	1.4 0.9	8° 0°

**Note**

1. Plastic or metal protrusions of 0.25 mm maximum per side are not included.

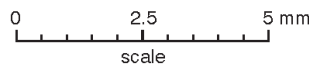
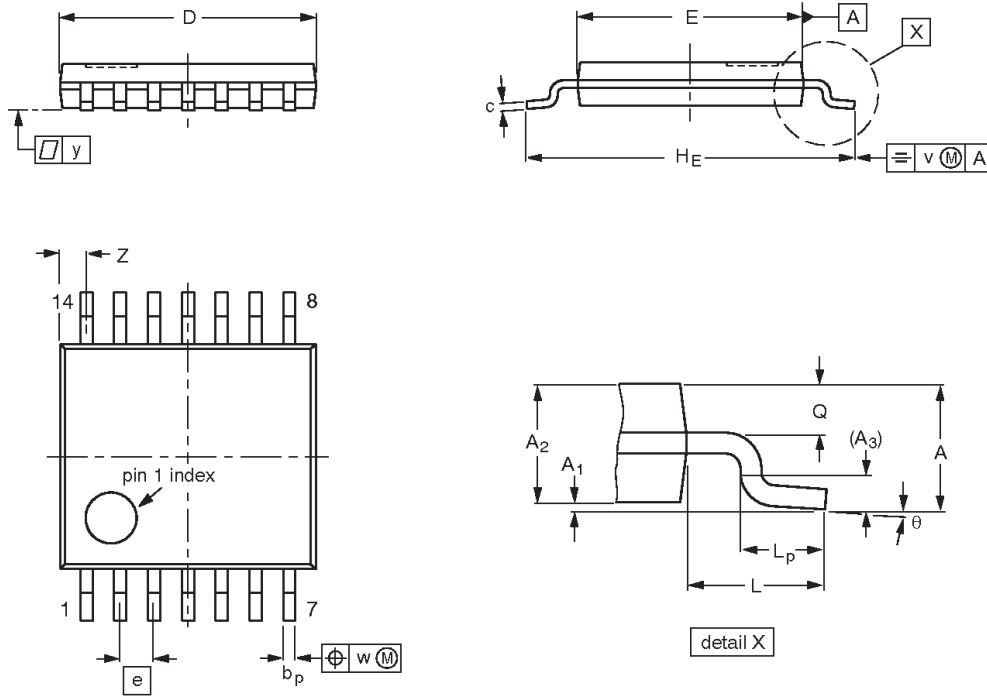
OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	EIAJ			
SOT337-1		MO-150				96-01-18 99-12-27

### 3.3 V Quad 2-input OR gate

74LVT32

TSSOP14: plastic thin shrink small outline package; 14 leads; body width 4.4 mm

SOT402-1



**DIMENSIONS (mm are the original dimensions)**

UNIT	A max.	A <sub>1</sub>	A <sub>2</sub>	A <sub>3</sub>	b <sub>p</sub>	c	D <sup>(1)</sup>	E <sup>(2)</sup>	e	H <sub>E</sub>	L	L <sub>p</sub>	Q	v	w	y	Z <sup>(1)</sup>	θ
mm	1.10	0.15 0.05	0.95 0.80	0.25	0.30 0.19	0.2 0.1	5.1 4.9	4.5 4.3	0.65	6.6 6.2	1.0	0.75 0.50	0.4 0.3	0.2	0.13	0.1	0.72 0.38	8° 0°

**Notes**

1. Plastic or metal protrusions of 0.15 mm maximum per side are not included.
2. Plastic interlead protrusions of 0.25 mm maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	EIAJ			
SOT402-1		MO-153				-95-04-04 99-12-27



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**3.3 V Quad 2-input OR gate****74LVT32**

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**REVISION HISTORY**

<b>Rev</b>	<b>Date</b>	<b>Description</b>
_2	2002 Sep 06	Product data (9397 750 10298); supersedes Product specification 74LVT32 of 1996 Aug 28. Modifications: There are no changes to any data. Document re-issued to improve quality of package outline drawings display only.
–	1996 Aug 28	Product specification; initial version. Engineering Change Notice: 853-1873 17244 (date: 1996 Aug 28).

## 3.3 V Quad 2-input OR gate

74LVT32

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Data sheet status <sup>[1]</sup>	Product status <sup>[2]</sup>	Definitions
Objective data	Development	This data sheet contains data from the objective specification for product development. Philips Semiconductors reserves the right to change the specification in any manner without notice.
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[2] The product status of the device(s) described in this data sheet may have changed since this data sheet was published. The latest information is available on the Internet at URL <http://www.semiconductors.philips.com>.

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