



Z86E30/E31/E40

Z8 4K OTP MICROCONTROLLER

FEATURES

| Device | ROM (KB) | RAM* (Bytes) | I/O Lines | Speed (MHz) |
|--------|----------|--------------|-----------|-------------|
| Z86E30 | 4 | 237 | 24 | 16 |
| Z86E31 | 2 | 125 | 24 | 16 |
| Z86E40 | 4 | 236 | 32 | 16 |

Note: *General-Purpose

- Standard Temperature ($V_{CC} = 3.5V$ to $5.5V$)
- Extended Temperature ($V_{CC} = 4.5V$ to $5.5V$)
- Available Packages:
28-Pin DIP/SOIC/PLCC OTP (Z86E30/31 only)
40-Pin DIP OTP (Z86E40 only)
44-Pin PLCC/LQFP OTP (Z86E40 only)
- Software Enabled Watch-Dog Timer (WDT)
- Push-Pull/Open-Drain Programmable on Port 0, Port 1, and Port 2
- 24/32 Input/Output Lines
- Auto Latches
- Auto Power-On Reset (POR)
- Programmable OTP Options:
RC Oscillator
EPROM Protect
Auto Latch Disable
Permanently Enabled WDT
Crystal Oscillator Feedback Resistor Disable
RAM Protect
- Low-Power Consumption: 60 mW
- Fast Instruction Pointer: 0.75 μs
- Two Standby Modes: STOP and HALT
- Digital Inputs CMOS Levels, Schmitt-Triggered
- Software Programmable Low EMI Mode
- Two Programmable 8-Bit Counter/Timers Each with a 6-Bit Programmable Prescaler
- Six Vectored, Priority Interrupts from Six Different Sources
- Two Comparators
- On-Chip Oscillator that Accepts a Crystal, Ceramic Resonator, LC, RC, or External Clock Drive

GENERAL DESCRIPTION

The Z86E30/E31/E40 8-Bit One-Time Programmable (OTP) Microcontrollers are members of Zilog's single-chip Z8[®] MCU family featuring enhanced wake-up circuitry, programmable Watch-Dog Timers, Low Noise EMI options, and easy hardware/software system expansion capability.

Four basic address spaces support a wide range of memory configurations. The designer has access to three additional control registers that allow easy access to register mapped peripheral and I/O circuits.

For applications demanding powerful I/O capabilities, the Z86E30/E31 have 24 pins, and the Z86E40 has 32 pins of dedicated input and output. These lines are grouped into four ports, eight lines per port, and are configurable under software control to provide timing, status signals, and parallel I/O with or without handshake, and address/data bus for interfacing external memory.

Notes: All signals with a preceding front slash, “/”, are active Low. For example, B/W (WORD is active Low); B/W (BYTE is active Low, only).

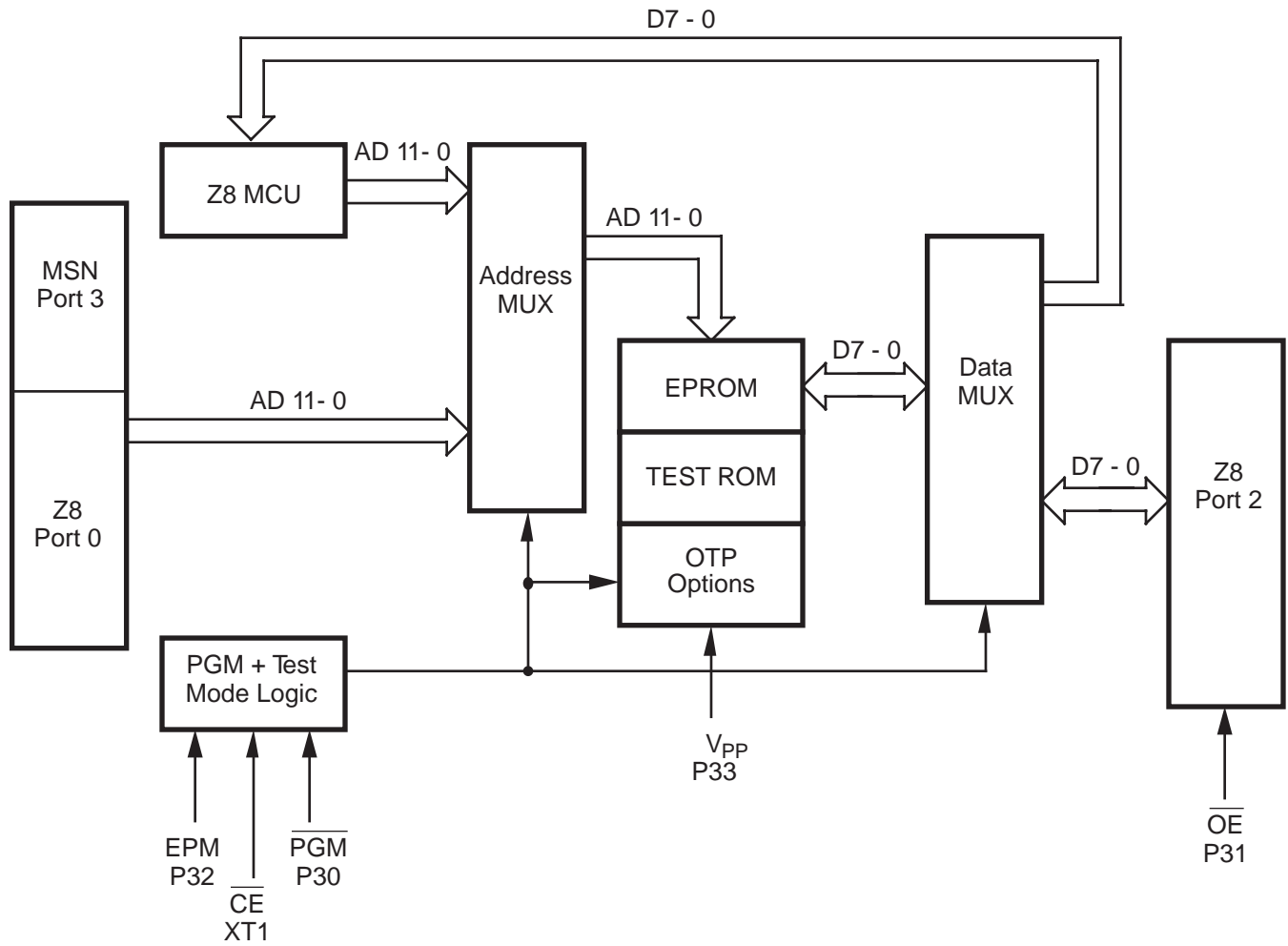


Figure 2. EPROM Programming Block Diagram

PIN IDENTIFICATION



Figure 3. 40-Pin DIP Pin Configuration Standard Mode

Table 1. 40-Pin DIP Pin Identification Standard Mode

| Pin # | Symbol | Function | Direction |
|-------|-----------------|------------------------|-----------|
| 1 | R/W | Read/Write | Output |
| 2–4 | P25–P27 | Port 2, Pins 5,6,7 | In/Output |
| 5–7 | P04–P06 | Port 0, Pins 4,5,6 | In/Output |
| 8–9 | P14–P15 | Port 1, Pins 4,5 | In/Output |
| 10 | P07 | Port 0, Pin 7 | In/Output |
| 11 | V _{CC} | Power Supply | |
| 12–13 | P16–P17 | Port 1, Pins 6,7 | In/Output |
| 14 | XTAL2 | Crystal Oscillator | Output |
| 15 | XTAL1 | Crystal Oscillator | Input |
| 16–18 | P31–P33 | Port 3, Pins 1,2,3 | Input |
| 19 | P34 | Port 3, Pin 4 | Output |
| 20 | AS | Address Strobe | Output |
| 21 | RESET | Reset | Input |
| 22 | P35 | Port 3, Pin 5 | Output |
| 23 | P37 | Port 3, Pin 7 | Output |
| 24 | P36 | Port 3, Pin 6 | Output |
| 25 | P30 | Port 3, Pin 0 | Input |
| 26–27 | P00–P01 | Port 0, Pins 0,1 | In/Output |
| 28–29 | P10–P11 | Port 1, Pins 0,1 | In/Output |
| 30 | P02 | Port 0, Pin 2 | In/Output |
| 31 | GND | Ground | |
| 32–33 | P12–P13 | Port 1, Pins 2,3 | In/Output |
| 34 | P03 | Port 0, Pin 3 | In/Output |
| 35–39 | P20–P24 | Port 2, Pins 0,1,2,3,4 | In/Output |
| 40 | DS | Data Strobe | Output |

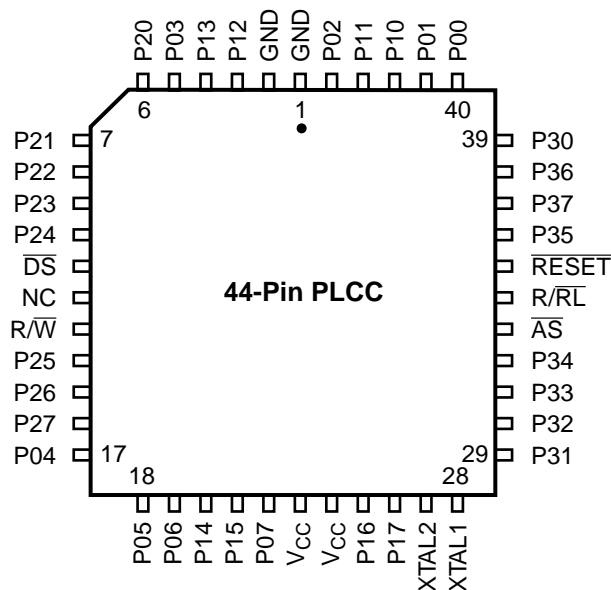


Figure 4. 44-Pin PLCC Pin Configuration
Standard Mode

Table 2. 44-Pin PLCC Pin Identification

| Pin # | Symbol | Function | Direction |
|-------|-----------------------------|------------------------|-----------|
| 1–2 | GND | Ground | |
| 3–4 | P12–P13 | Port 1, Pins 2,3 | In/Output |
| 5 | P03 | Port 0, Pin 3 | In/Output |
| 6–10 | P20–P24 | Port 2, Pins 0,1,2,3,4 | In/Output |
| 11 | \overline{DS} | Data Strobe | Output |
| 12 | NC | No Connection | |
| 13 | $\overline{R/\overline{W}}$ | Read/Write | Output |
| 14–16 | P25–P27 | Port 2, Pins 5,6,7 | In/Output |
| 17–19 | P04–P06 | Port 0, Pins 4,5,6 | In/Output |
| 20–21 | P14–P15 | Port 1, Pins 4,5 | In/Output |
| 22 | P07 | Port 0, Pin 7 | In/Output |
| 23–24 | V_{CC} | Power Supply | |
| 25–26 | P16–P17 | Port 1, Pins 6,7 | In/Output |
| 27 | XTAL2 | Crystal Oscillator | Output |
| 28 | XTAL1 | Crystal Oscillator | Input |
| 29–31 | P31–P33 | Port 3, Pins 1,2,3 | Input |
| 32 | P34 | Port 3, Pin 4 | Output |

Table 2. 44-Pin PLCC Pin Identification

| Pin # | Symbol | Function | Direction |
|-------|------------------------------|--------------------|-----------|
| 33 | \overline{AS} | Address Strobe | Output |
| 34 | $\overline{R/\overline{RL}}$ | ROM/ROMless select | Input |
| 35 | \overline{RESET} | Reset | Input |
| 36 | P35 | Port 3, Pin 5 | Output |
| 37 | P37 | Port 3, Pin 7 | Output |
| 38 | P36 | Port 3, Pin 6 | Output |
| 39 | P30 | Port 3, Pin 0 | Input |
| 40–41 | P00–P01 | Port 0, Pins 0,1 | In/Output |
| 42–43 | P10–P11 | Port 1, Pins 0,1 | In/Output |
| 44 | P02 | Port 0, Pin 2 | In/Output |

PIN IDENTIFICATION (Continued)

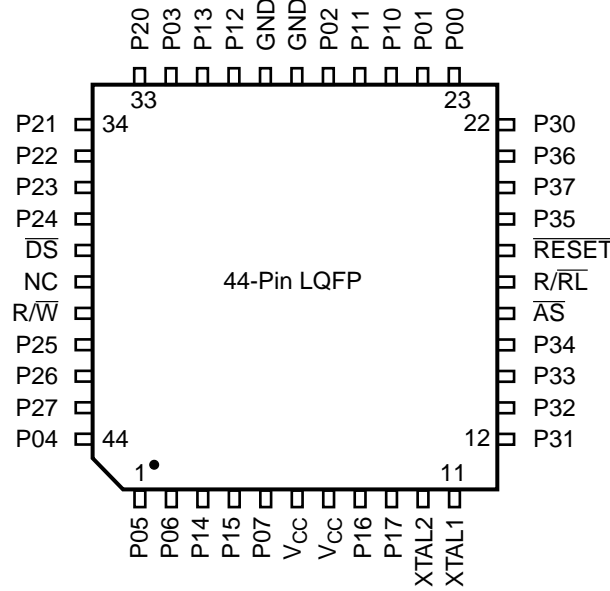


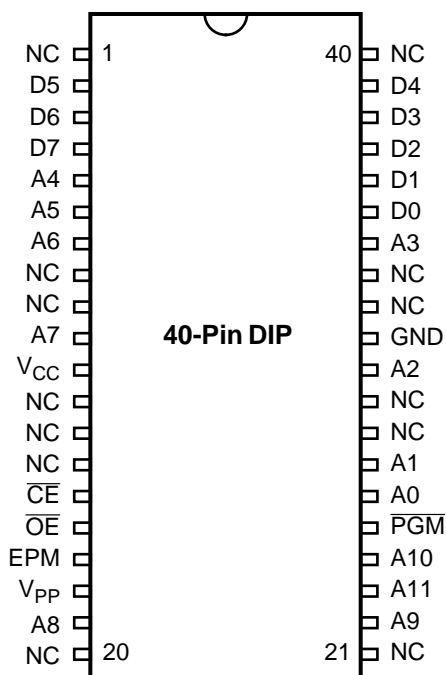
Figure 5. 44-Pin LQFP Pin Configuration
Standard Mode

Table 3. 44-Pin LQFP Pin Identification

| Pin # | Symbol | Function | Direction |
|-------|-----------------|--------------------|-----------|
| 1–2 | P05–P06 | Port 0, Pins 5,6 | In/Output |
| 3–4 | P14–P15 | Port 1, Pins 4,5 | In/Output |
| 5 | P07 | Port 0, Pin 7 | In/Output |
| 6–7 | V _{CC} | Power Supply | |
| 8–9 | P16–P17 | Port 1, Pins 6,7 | In/Output |
| 10 | XTAL2 | Crystal Oscillator | Output |
| 11 | XTAL1 | Crystal Oscillator | Input |
| 12–14 | P31–P33 | Port 3, Pins 1,2,3 | Input |
| 15 | P34 | Port 3, Pin 4 | Output |
| 16 | AS | Address Strobe | Output |
| 17 | R/RL | ROM/ROMless select | Input |
| 18 | RESET | Reset | Input |
| 19 | P35 | Port 3, Pin 5 | Output |
| 20 | P37 | Port 3, Pin 7 | Output |
| 21 | P36 | Port 3, Pin 6 | Output |
| 22 | P30 | Port 3, Pin 0 | Input |
| 23–24 | P00–P01 | Port 0, Pin 0,1 | In/Output |
| 25–26 | P10–P11 | Port 1, Pins 0,1 | In/Output |

Table 3. 44-Pin LQFP Pin Identification

| Pin # | Symbol | Function | Direction |
|-------|---------|------------------------|-----------|
| 27 | P02 | Port 0, Pin 2 | In/Output |
| 28–29 | GND | Ground | |
| 30–31 | P12–P13 | Port 1, Pins 2,3 | In/Output |
| 32 | P03 | Port 0, Pin 3 | In/Output |
| 33–37 | P20–4 | Port 2, Pins 0,1,2,3,4 | In/Output |
| 38 | DS | Data Strobe | Output |
| 39 | NC | No Connection | |
| 40 | R/W | Read/Write | Output |
| 41–43 | P25–P27 | Port 2, Pins 5,6,7 | In/Output |
| 44 | P04 | Port 0, Pin 4 | In/Output |



**Figure 6. 40-Pin DIP Pin Configuration
EPROM Mode**

**Table 4. 40-Pin DIP Package Pin Identification
EPROM Mode**

| Pin # | Symbol | Function | Direction |
|-------|------------------|------------------|-----------|
| 1 | NC | No Connection | |
| 2–4 | D5–D7 | Data 5,6,7 | In/Output |
| 5–7 | A4–A6 | Address 4,5,6 | Input |
| 8–9 | NC | No Connection | |
| 10 | A7 | Address 7 | Input |
| 11 | V _{CC} | Power Supply | |
| 12–14 | NC | No Connection | |
| 15 | \overline{CE} | Chip Select | Input |
| 16 | \overline{OE} | Output Enable | Input |
| 17 | EPM | EPROM Prog. Mode | Input |
| 18 | V _{PP} | Prog. Voltage | Input |
| 19 | A8 | Address 8 | Input |
| 20–21 | NC | No Connection | |
| 22 | A9 | Address 9 | Input |
| 23 | A11 | Address 11 | Input |
| 24 | A10 | Address 10 | Input |
| 25 | \overline{PGM} | Prog. Mode | Input |
| 26–27 | A0–A1 | Address 0,1 | Input |
| 28–29 | NC | No Connection | |
| 30 | A2 | Address 2 | Input |
| 31 | GND | Ground | |
| 32–33 | NC | No Connection | |
| 34 | A3 | Address 3 | Input |
| 35–39 | D0–D4 | Data 0,1,2,3,4 | In/Output |
| 40 | NC | No Connection | |

PIN IDENTIFICATION (Continued)



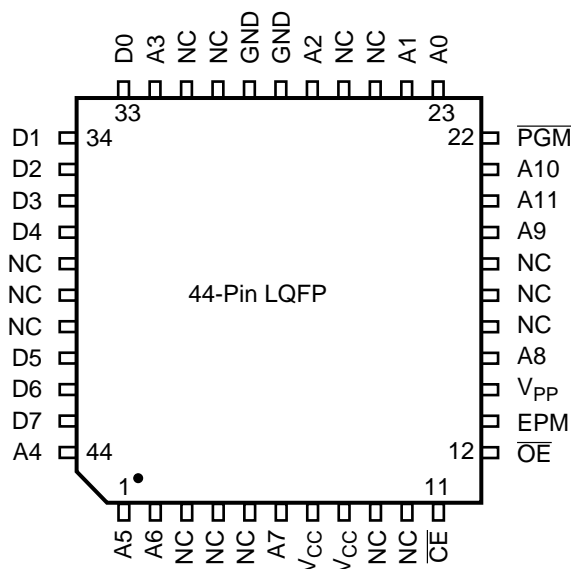
**Figure 7. 44-Pin PLCC Pin Configuration
EPROM Programming Mode**

**Table 5. 44-Pin PLCC Pin Configuration
EPROM Programming Mode**

| Pin # | Symbol | Function | Direction |
|-------|-----------------|------------------|-----------|
| 1–2 | GND | Ground | |
| 3–4 | NC | No Connection | |
| 5 | A3 | Address 3 | Input |
| 6–10 | D0–D4 | Data 0,1,2,3,4 | In/Output |
| 11–13 | NC | No Connection | |
| 14–16 | D5–D7 | Data 5,6,7 | In/Output |
| 17–19 | A4–A6 | Address 4,5,6 | Input |
| 20–21 | NC | No Connection | |
| 22 | A7 | Address 7 | Input |
| 23–24 | V _{CC} | Power Supply | |
| 25–27 | NC | No Connection | |
| 28 | \overline{CE} | Chip Select | Input |
| 29 | \overline{OE} | Output Enable | Input |
| 30 | EPM | EPROM Prog. Mode | Input |

**Table 5. 44-Pin PLCC Pin Configuration
EPROM Programming Mode**

| Pin # | Symbol | Function | Direction |
|-------|------------------|---------------|-----------|
| 31 | V _{PP} | Prog. Voltage | Input |
| 32 | A8 | Address 8 | Input |
| 33–35 | NC | No Connection | |
| 36 | A9 | Address 9 | Input |
| 37 | A11 | Address 11 | Input |
| 38 | A10 | Address 10 | Input |
| 39 | \overline{PGM} | Prog. Mode | Input |
| 40–41 | A0,A1 | Address 0,1 | Input |
| 42–43 | NC | No Connection | |
| 44 | A2 | Address 2 | Input |



**Figure 8. 44-Pin LQFP Pin Configuration
EPROM Programming Mode**

**Table 6. 44-Pin LQFP Pin Configuration
EPROM Programming Mode**

| Pin # | Symbol | Function | Direction |
|-------|------------------|------------------|-----------|
| 1–2 | A5–A6 | Address 5,6 | Input |
| 3–4 | NC | No Connection | |
| 5 | A7 | Address 7 | Input |
| 6–7 | V _{CC} | Power Supply | |
| 8–10 | NC | No Connection | |
| 11 | \overline{CE} | Chip Select | Input |
| 12 | \overline{OE} | Output Enable | Input |
| 13 | EPM | EPROM Prog. Mode | Input |
| 14 | V _{PP} | Prog. Voltage | Input |
| 15 | A8 | Address 8 | Input |
| 16–18 | NC | No Connection | |
| 19 | A9 | Address 9 | Input |
| 20 | A11 | Address 11 | Input |
| 21 | A10 | Address 10 | Input |
| 22 | \overline{PGM} | Prog. Mode | Input |

**Table 6. 44-Pin LQFP Pin Configuration
EPROM Programming Mode**

| Pin # | Symbol | Function | Direction |
|-------|--------|----------------|-----------|
| 23–24 | A0,A1 | Address 0,1 | Input |
| 25–26 | NC | No Connection | |
| 27 | A2 | Address 2 | Input |
| 28–29 | GND | Ground | |
| 30–31 | NC | No Connection | |
| 32 | A3 | Address 3 | Input |
| 33–37 | D0–D4 | Data 0,1,2,3,4 | In/Output |
| 38–40 | NC | No Connection | |
| 41–43 | D5–D7 | Data 5,6,7 | In/Output |
| 44 | A4 | Address 4 | Input |

PIN IDENTIFICATION (Continued)



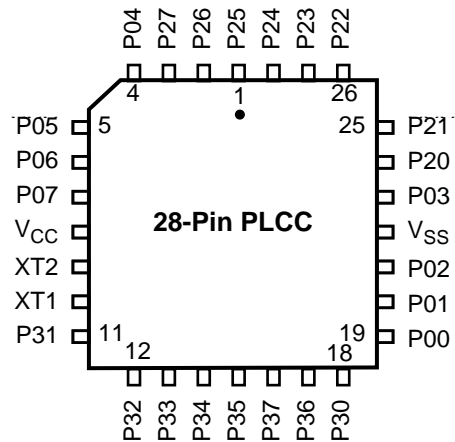
**Figure 9. Standard Mode
28-Pin DIP/SOIC Pin Configuration**



**Figure 10. EPROM Programming Mode
28-Pin DIP/SOIC Pin Configuration**

**Table 7. 28-Pin DIP/SOIC/PLCC
Pin Identification***

| Pin # | Symbol | Function | Direction |
|-------|-----------------|---------------------------|-----------|
| 1–3 | P25–P27 | Port 2, Pins 5,6, | In/Output |
| 4–7 | P04–P07 | Port 0, Pins 4,5,6,7 | In/Output |
| 8 | V _{CC} | Power Supply | |
| 9 | XTAL2 | Crystal Oscillator | Output |
| 10 | XTAL1 | Crystal Oscillator | Input |
| 11–13 | P31–P33 | Port 3, Pins 1,2,3 | Input |
| 14–15 | P34–P35 | Port 3, Pins 4,5 | Output |
| 16 | P37 | Port 3, Pin 7 | Output |
| 17 | P36 | Port 3, Pin 6 | Output |
| 18 | P30 | Port 3, Pin 0 | Input |
| 19–21 | P00–P02 | Port 0, Pins 0,1,2 | In/Output |
| 22 | V _{SS} | Ground | |
| 23 | P03 | Port 0, Pin 3 | In/Output |
| 24–28 | P20–P24 | Port 2, Pins 0,1,2,3,4 | In/Output |



**Figure 11. Standard Mode
28-Pin PLCC Pin Configuration**



**Figure 12. EPROM Programming Mode
28-Pin PLCC Pin Configuration**

**Table 8. 28-Pin EPROM
Pin Identification**

| Pin # | Symbol | Function | Direction |
|-------|------------------|------------------|-----------|
| 1–3 | D5–D7 | Data 5,6,7 | In/Output |
| 4–7 | A4–A7 | Address 4,5,6,7 | Input |
| 8 | V _{CC} | Power Supply | |
| 9 | NC | No connection | |
| 10 | \overline{CE} | Chip Select | Input |
| 11 | \overline{OE} | Output Enable | Input |
| 12 | EPM | EPROM Prog. Mode | Input |
| 13 | V _{PP} | Prog. Voltage | Input |
| 14–15 | A8–A9 | Address 8,9 | Input |
| 16 | A11 | Address 11 | Input |
| 17 | A10 | Address 10 | Input |
| 18 | \overline{PGM} | Prog. Mode | Input |
| 19–21 | A0–A2 | Address 0,1,2 | Input |
| 22 | V _{SS} | Ground | |
| 23 | A3 | Address 3 | Input |
| 24–28 | D0–D4 | Data 0,1,2,3,4 | In/Output |

ABSOLUTE MAXIMUM RATINGS

| Parameter | Min | Max | Units |
|--|------|------------|---------|
| Ambient Temperature under Bias | -40 | +105 | C |
| Storage Temperature | -65 | +150 | C |
| Voltage on any Pin with Respect to V_{SS} [Note 1] | -0.6 | +7 | V |
| Voltage on V_{DD} Pin with Respect to V_{SS} | -0.3 | +7 | V |
| Voltage on XTAL1 and \overline{RESET} Pins with Respect to V_{SS} [Note 2] | -0.6 | $V_{DD}+1$ | V |
| Total Power Dissipation | | 1.21 | W |
| Maximum Allowable Current out of V_{SS} | | 220 | mA |
| Maximum Allowable Current into V_{DD} | | 180 | mA |
| Maximum Allowable Current into an Input Pin [Note 3] | -600 | +600 | μ A |
| Maximum Allowable Current into an Open-Drain Pin [Note 4] | -600 | +600 | μ A |
| Maximum Allowable Output Current Sunked by Any I/O Pin | | 25 | mA |
| Maximum Allowable Output Current Sourced by Any I/O Pin | | 25 | mA |
| Maximum Allowable Output Current Sunked by \overline{RESET} Pin | | 3 mA | |

Notes:

1. This applies to all pins except XTAL pins and where otherwise noted.
2. There is no input protection diode from pin to V_{DD} .
3. This excludes XTAL pins.
4. Device pin is not at an output Low state.

Stresses greater than those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only; functional operation of the device at any condition above those indicated in the operational sections of these specifications is not implied. Exposure to absolute maximum rating conditions for an extended period may affect device reliability.

Total power dissipation should not exceed 1.2 W for the package. Power dissipation is calculated as follows:

$$\begin{aligned} \text{Total Power Dissipation} = & V_{DD} \times [I_{DD} - (\text{sum of } I_{OH})] \\ & + \text{sum of } [(V_{DD} - V_{OH}) \times I_{OH}] \\ & + \text{sum of } (V_{OL} \times I_{OL}) \end{aligned}$$

STANDARD TEST CONDITIONS

The characteristics listed below apply for standard test conditions as noted. All voltages are referenced to Ground. Positive current flows into the referenced pin (Test Load).



Figure 13. Test Load Diagram

CAPACITANCE

$T_A = 25^\circ\text{C}$, $V_{CC} = \text{GND} = 0\text{V}$, $f = 1.0\text{ MHz}$; unmeasured pins returned to GND.

| Parameter | Min | Max |
|--------------------|-----|-------|
| Input capacitance | 0 | 12 pF |
| Output capacitance | 0 | 12 pF |
| I/O capacitance | 0 | 12 pF |

DC ELECTRICAL CHARACTERISTICS

| $T_A = 0^\circ\text{C to } +70^\circ\text{C}$ | | | | | | | | |
|---|-------------------------------------|----------------------|-------------------|-----------------------|-------------------|---------------|--|-------|
| Sym | Parameter | V_{CC} Note [3] | Min | Max | Typical @ 25°C | Units | Conditions | Notes |
| V_{CH} | Clock Input High Voltage | 3.5V | $0.7 V_{CC}$ | $V_{CC}+0.3$ | 1.8 | V | Driven by External Clock Generator | |
| | | 5.5V | $0.7 V_{CC}$ | $V_{CC}+0.3$ | 2.5 | V | | |
| V_{CL} | Clock Input Low Voltage | 3.5V | $\text{GND} -0.3$ | $0.2 V_{CC}$ | 0.9 | V | Driven by External Clock Generator | |
| | | 4.5V | $\text{GND} -0.3$ | $0.2 V_{CC}$ | 1.5 | V | | |
| V_{IH} | Input High Voltage | 3.5V | $0.7 V_{CC}$ | $V_{CC}+0.3$ | 2.5 | V | | |
| | | 5.5V | $0.7 V_{CC}$ | $V_{CC}+0.3$ | 2.5 | V | | |
| V_{IL} | Input Low Voltage | 3.5V | $\text{GND} -0.3$ | $0.2 V_{CC}$ | 1.5 | V | | |
| | | 5.5V | $\text{GND} -0.3$ | $0.2 V_{CC}$ | 1.5 | V | | |
| V_{OH} | Output High Voltage Low EMI Mode | 3.5V | $V_{CC} -0.4$ | | 3.3 | V | $I_{OH} = -0.5\text{ mA}$ | |
| | | 5.5V | $V_{CC} -0.4$ | | 4.8 | V | | |
| V_{OH1} | Output High Voltage | 3.5V | $V_{CC} -0.4$ | | 3.3 | V | $I_{OH} = -2.0\text{ mA}$ $I_{OH} = -2.0\text{ mA}$ | |
| | | 5.5V | $V_{CC} -0.4$ | | 4.8 | V | | |
| V_{OL} | Output Low Voltage Low EMI Mode | 3.5V | | 0.4 | 0.2 | V | $I_{OL} = 1.0\text{ mA}$ $I_{OL} = 1.0\text{ mA}$ | |
| | | 4.5V | | 0.4 | 0.2 | V | | |
| V_{OL1} | Output Low Voltage | 3.5V | | 0.4 | 0.1 | V | $I_{OL} = +4.0\text{ mA}$ $I_{OL} = +4.0\text{ mA}$ | 8 |
| | | 4.5V | | 0.4 | 0.1 | V | | |
| V_{OL2} | Output Low Voltage | 3.5V | | 1.2 | 0.5 | V | $I_{OL} = +12\text{ mA}$ $I_{OL} = +12\text{ mA}$ | 8 |
| | | 4.5V | | 1.2 | 0.5 | V | | |
| V_{RH} | Reset Input High Voltage | 3.5V | $.8 V_{CC}$ | V_{CC} | 1.7 | V | | |
| | | 5.5V | $.8 V_{CC}$ | V_{CC} | 2.1 | V | | |
| V_{RL} | Reset Input Low Voltage | 3.5V | $\text{GND} -0.3$ | $0.2 V_{CC}$ | 1.3 | V | | 13 |
| | | 5.5V | $\text{GND} -0.3$ | $0.2 V_{CC}$ | 1.7 | V | | |
| V_{OLR} | Reset Output Low Voltage | 3.5V | | 0.6 | 0.3 | V | $I_{OL} = 1.0\text{ mA}$ $I_{OL} = 1.0\text{ mA}$ | |
| | | 5.5V | | 0.6 | 0.2 | V | | |
| V_{OFFSET} | Comparator Input Offset Voltage | 3.5V | | 25 | 10 | mV | | |
| | | 4.5V | | 25 | 10 | mV | | |
| V_{ICR} | Input Common Mode Voltage Range | 3.5V | 0 | $V_{CC} -1.0\text{V}$ | | V | | 10 |
| | | 5.5V | 0 | $V_{CC} -1.0\text{V}$ | | V | | |
| I_{IL} | Input Leakage | 3.5V | -1 | 2 | 0.032 | μA | $V_{IN} = 0\text{V}$, V_{CC} | |
| | | 4.5V | -1 | 2 | 0.032 | μA | | |
| I_{OL} | Output Leakage | 3.5V | -1 | 2 | 0.032 | μA | $V_{IN} = 0\text{V}$, V_{CC} | |
| | | 4.5V | -1 | 2 | 0.032 | μA | | |
| I_{IR} | Reset Input Current | 3.5V | -20 | -130 | -65 | μA | | |
| | | 4.5V | -20 | -180 | -112 | μA | | |

DC ELECTRICAL CHARACTERISTICS (Continued)

| T _A = 0 °C to +70 °C | | | | | | | | |
|---------------------------------|--------------------|-----------------------------|------|-----|-------------------|-------|--|-------------|
| Sym | Parameter | V _{CC} Note [3] | Min | Max | Typical @ 25°C | Units | Conditions | Notes |
| I _{CC} | Supply Current | 3.5V | | 20 | 7 | mA | @ 16 MHz | 4,5 |
| | | 5.5V | | 25 | 20 | mA | @ 16 MHz | 4,5 |
| I _{CC1} | Standby Current | 3.5V | | 8 | 3.7 | mA | V _{IN} = 0V, V _{CC} | 4,5 |
| | | 5.5V | | 8 | 3.7 | mA | @ 16 MHz | 4,5 |
| | Halt Mode | 3.5V | | 7.0 | 2.9 | mA | Clock Divide by | 4,5 |
| | | 5.5V | | 7.0 | 2.9 | mA | 16 @ 16 MHz | 4,5 |
| I _{CC2} | Standby Current | 3.5V | | 10 | 2 | μA | V _{IN} = 0V, V _{CC} | 6,11 |
| | | 5.5V | | 10 | 3 | μA | V _{IN} = 0V, V _{CC} | 6,11 |
| | Stop Mode | 3.5V | | 800 | 600 | μA | V _{IN} = 0V, V _{CC} | 6,11,1 4 |
| | | 5.5V | | 800 | 600 | μA | V _{IN} = 0V, V _{CC} | 6,11,1 4 |
| | | | | | | | | |
| I _{ALL} | Auto Latch | 3.5V | 0.7 | 8 | 2.4 | μA | 0V < V _{IN} < V _{CC} | 9 |
| | Low Current | 5.5V | 1.4 | 15 | 4.7 | μA | 0V < V _{IN} < V _{CC} | 9 |
| I _{ALH} | Auto Latch | 3.5V | -0.6 | -5 | -1.8 | μA | 0V < V _{IN} < V _{CC} | 9 |
| | High Current | 5.5V | -1 | -8 | -3.8 | μA | 0V < V _{IN} < V _{CC} | 9 |
| T _{POR} | Power On Reset | 3.5V | 3.0 | 24 | 7 | ms | | |
| | | 5.5V | 2.0 | 13 | 4 | ms | | |
| V _{LV} | Auto Reset Voltage | | 2.3 | 3.1 | 2.9 | V | | 1,7 |

Notes:

1. Device does function down to the Auto Reset voltage.
2. GND=0V
3. The V_{CC} voltage specification of 5.5V guarantees 5.0V ± 0.5V and the V_{CC} voltage specification of 3.5V guarantees only 3.5V.
4. All outputs unloaded, I/O pins floating, inputs at rail.
5. CL1= CL2 = 22 pF
6. Same as note [4] except inputs at V_{CC}.
7. Max. temperature is 70°C.
8. STD Mode (not Low EMI Mode)
9. Auto Latch (mask option) selected
10. For analog comparator inputs when analog comparators are enabled.
11. Clock must be forced Low, when XTAL1 is clock driven and XTAL2 is floating.
12. Typicals are at V_{CC} = 5.0V and V_{CC} = 3.5V
13. Z86E40 only
14. WDT running

| $T_A = -40\text{ }^{\circ}\text{C to } +105\text{ }^{\circ}\text{C}$ | | | | | | | | |
|--|----------------------------------|-----------------------------|----------------------|-----------------------|-------------------|-------|---|---------|
| Sym | Parameter | V _{CC} Note [3] | Min | Max | Typical @ 25°C | Units | Conditions | Notes |
| V _{CH} | Clock Input High Voltage | 4.5V | 0.7 V _{CC} | V _{CC} +0.3 | 2.5 | V | Driven by External Clock Generator | |
| | | 5.5V | 0.7 V _{CC} | V _{CC} +0.3 | 2.5 | V | | |
| V _{CL} | Clock Input Low Voltage | 4.5V | GND-0.3 | 0.2 V _{CC} | 1.5 | V | Driven by External Clock Generator | |
| | | 5.5V | GND-0.3 | 0.2 V _{CC} | 1.5 | V | | |
| V _{IH} | Input High Voltage | 4.5V | 0.7 V _{CC} | V _{CC} +0.3 | 2.5 | V | | |
| | | 5.5V | 0.7 V _{CC} | V _{CC} +0.3 | 2.5 | V | | |
| V _{IL} | Input Low Voltage | 4.5V | GND-0.3 | 0.2 V _{CC} | 1.5 | V | | |
| | | 5.5V | GND-0.3 | 0.2 V _{CC} | 1.5 | V | | |
| V _{OH} | Output High Voltage Low EMI Mode | 4.5V | V _{CC} -0.4 | | 4.8 | V | I _{OH} = -0.5 mA | 8 |
| | | 5.5V | V _{CC} -0.4 | | 4.8 | V | I _{OH} = -0.5 mA | 8 |
| V _{OH1} | Output High Voltage | 4.5V | V _{CC} -0.4 | | 4.8 | V | I _{OH} = -2.0 mA | 8 |
| | | 4.5V | V _{CC} -0.4 | | 4.8 | V | I _{OH} = -2.0 mA | 8 |
| V _{OL} | Output Low Voltage Low EMI Mode | 4.5V | | 0.4 | 0.2 | V | I _{OL} = 1.0 mA | |
| | | 5.5V | | 0.4 | 0.2 | V | I _{OL} = 1.0 mA | |
| V _{OL1} | Output Low Voltage | 4.5V | | 0.4 | 0.1 | V | I _{OL} = +4.0 mA | 8 |
| | | 5.5V | | 0.4 | 0.1 | V | I _{OL} = +4.0 mA | 8 |
| V _{OL2} | Output Low Voltage | 4.5V | | 1.2 | 0.5 | V | I _{OL} = +12 mA | 8 |
| | | 5.5V | | 1.2 | 0.5 | V | I _{OL} = +12 mA | 8 |
| V _{RH} | Reset Input High Voltage | 3.5V | .8 V _{CC} | V _{CC} | 1.7 | V | | 13 |
| | | 5.5V | .8 V _{CC} | V _{CC} | 2.1 | V | | 13 |
| V _{OLR} | Reset Output Low Voltage | 3.5V | | 0.6 | 0.3 | V | I _{OL} = 1.0 mA | 13 |
| | | 5.5V | | 0.6 | 0.2 | V | I _{OL} = 1.0 mA | 13 |
| V _{OFFSET} | Comparator Input Offset Voltage | 4.5V | | 25 | 10 | mV | | |
| | | 5.5V | | 25 | 10 | mV | | |
| V _{ICR} | Input Common Mode Voltage Range | 4.5V | 0 | V _{CC} -1.5V | | V | | 10 |
| | | 5.5V | 0 | V _{CC} -1.5V | | V | | 10 |
| I _{IL} | Input Leakage | 4.5V | -1 | 2 | <1 | μA | V _{IN} = 0V, V _{CC} | |
| | | 5.5V | -1 | 2 | <1 | μA | V _{IN} = 0V, V _{CC} | |
| I _{OL} | Output Leakage | 4.5V | -1 | 2 | <1 | μA | V _{IN} = 0V, V _{CC} | |
| | | 5.5V | -1 | 2 | <1 | μA | V _{IN} = 0V, V _{CC} | |
| I _{IR} | Reset Input Current | 4.5V | -18 | -180 | -112 | μA | | |
| | | 5.5V | -18 | -180 | -112 | μA | | |
| I _{CC} | Supply Current | 4.5V | | 25 | 20 | mA | @ 16 MHz | 4,5 |
| | | 5.5V | | 25 | 20 | mA | @ 16 MHz | 4,5 |
| I _{CC1} | Standby Current Halt Mode | 4.5V | | 8 | 3.7 | mA | V _{IN} = 0V, V _{CC} @ 16 MHz | 4,5 |
| | | 5.5V | | 8 | 3.7 | mA | V _{IN} = 0V, V _{CC} @ 16 MHz | 4,5 |
| I _{CC2} | Standby Current (Stop Mode) | 4.5V | | 10 | 2 | μA | V _{IN} = 0V, V _{CC} | 6,11,14 |
| | | 5.5V | | 10 | 3 | μA | V _{IN} = 0V, V _{CC} | 6,11,14 |
| I _{ALL} | Auto Latch Low Current | 4.5V | 1.4 | 20 | 4.7 | μA | 0V < V _{IN} < V _{CC} | 9 |
| | | 5.5V | 1.4 | 20 | 4.7 | μA | 0V < V _{IN} < V _{CC} | 9 |

DC ELECTRICAL CHARACTERISTICS (Continued)

| $T_A = -40\text{ }^\circ\text{C to } +105\text{ }^\circ\text{C}$ | | | | | | | | |
|--|--------------------|----------------------|------|-----|-------------------|---------------|-------------------------------|-------|
| Sym | Parameter | V_{CC} Note [3] | Min | Max | Typical @ 25°C | Units | Conditions | Notes |
| I_{ALH} | Auto Latch High | 4.5V | -1.0 | -10 | -3.8 | μA | $0\text{V} < V_{IN} < V_{CC}$ | 9 |
| | Current | 5.5V | -1.0 | -10 | -3.8 | μA | $0\text{V} < V_{IN} < V_{CC}$ | 9 |
| T_{POR} | Power On Reset | 4.5V | 2.0 | 14 | 4 | mS | | |
| | | 5.5V | 2.0 | 14 | 4 | mS | | |
| V_{LV} | Auto Reset Voltage | | 2.0 | 3.3 | 2.9 | V | | 1 |

1. Device does function down to the Auto Reset voltage.
2. GND=0V
3. The V_{CC} voltage specification of 5.5V guarantees $5.0\text{V} \pm 0.5\text{V}$.
4. All outputs unloaded, I/O pins floating, inputs at rail.
5. CL1= CL2 = 22 pF
6. Same as note [4] except inputs at V_{CC} .
7. Maximum temperature is 70°C
8. STD Mode (not Low EMI Mode)
9. Auto Latch (mask option) selected
10. For analog comparator inputs when analog comparators are enabled.
11. Clock must be forced Low, when XTAL1 is clock driven and XTAL2 is floating.
12. Typicals are at $V_{CC} = 5.0\text{V}$
13. Z86E40 only
14. WDT is not running.



Figure 14. External I/O or Memory Read/Write Timing
Z86E40 Only

DC ELECTRICAL CHARACTERISTICS (Continued)

| | | | | $T_A = 0^\circ\text{C to } 70^\circ\text{C}$ | | | |
|----|-----------|--|----------------------|--|-----|-------|-------|
| | | | | 16 MHz | | | |
| No | Symbol | Parameter | Note [3] V_{CC} | Min | Max | Units | Notes |
| 1 | TdA(AS) | Address Valid to \overline{AS} Rise Delay | 3.5V | 25 | | ns | 2 |
| | | | 5.5V | 25 | | ns | |
| 2 | TdAS(A) | \overline{AS} Rise to Address Float Delay | 3.5V | 35 | | ns | 2 |
| | | | 5.5V | 35 | | ns | |
| 3 | TdAS(DR) | \overline{AS} Rise to Read Data Req'd Valid | 3.5V | | 180 | ns | 1,2 |
| | | | 5.5V | | 180 | ns | |
| 4 | TwAS | \overline{AS} Low Width | 3.5V | 40 | | ns | 2 |
| | | | 5.5V | 40 | | ns | |
| 5 | TdAS(DS) | Address Float to \overline{DS} Fall | 3.5V | 0 | | ns | |
| | | | 5.5V | 0 | | ns | |
| 6 | TwDSR | \overline{DS} (Read) Low Width | 3.5V | 135 | | ns | 1,2 |
| | | | 5.5V | 135 | | ns | |
| 7 | TwDSW | \overline{DS} (Write) Low Width | 3.5V | 80 | | ns | 1,2 |
| | | | 5.5V | 80 | | ns | |
| 8 | TdDSR(DR) | \overline{DS} Fall to Read Data Req'd Valid | 3.5V | | 75 | ns | 1,2 |
| | | | 5.5V | | 75 | ns | |
| 9 | ThDR(DS) | Read Data to \overline{DS} Rise Hold Time | 3.5V | 0 | | ns | 2 |
| | | | 5.5V | 0 | | ns | |
| 10 | TdDS(A) | \overline{DS} Rise to Address Active Delay | 3.5V | 50 | | ns | 2 |
| | | | 5.5V | 50 | | ns | |
| 11 | TdDS(AS) | \overline{DS} Rise to \overline{AS} Fall Delay | 3.5V | 35 | | ns | 2 |
| | | | 5.5V | 35 | | ns | |
| 12 | TdR/W(AS) | R/ \overline{W} Valid to \overline{AS} Rise Delay | 3.5V | 25 | | ns | 2 |
| | | | 5.5V | 25 | | ns | |
| 13 | TdDS(R/W) | \overline{DS} Rise to R/ \overline{W} Not Valid | 3.5V | 35 | | ns | 2 |
| | | | 5.5V | 35 | | ns | |
| 14 | TdDW(DSW) | Write Data Valid to \overline{DS} Fall (Write) Delay | 3.5V | 55 | 25 | ns | 2 |
| | | | 5.5V | 55 | 25 | ns | |
| 15 | TdDS(DW) | \overline{DS} Rise to Write Data Not Valid Delay | 3.5V | 35 | | ns | 2 |
| | | | 5.5V | 35 | | ns | |
| 16 | TdA(DR) | Address Valid to Read Data Req'd Valid | 3.5V | | 230 | ns | 1,2 |
| | | | 5.5V | | 230 | ns | |
| 17 | TdAS(DS) | \overline{AS} Rise to \overline{DS} Fall Delay | 3.5V | 45 | | ns | 2 |
| | | | 5.5V | 45 | | ns | |
| 18 | TdDM(AS) | \overline{DM} Valid to \overline{AS} Fall Delay | 3.5V | 30 | | ns | 2 |
| | | | 5.5V | 30 | | ns | |
| 20 | ThDS(AS) | \overline{DS} Valid to Address Valid Hold Time | 3.5V | 35 | | ns | |
| | | | 5.5V | 35 | | ns | |

Notes:

1. When using extended memory timing, add 2 TpC.
2. Timing numbers given are for minimum TpC.
3. The V_{CC} voltage specification of 5.5V guarantees 5.0V $\pm 0.5V$ and the V_{CC} voltage specification of 3.5V guarantees only 3.5V

Standard Test Load

All timing references use 0.7 V_{CC} for a logic 1 and 0.2 V_{CC} for a logic 0.
For Standard Mode (not Low-EMI Mode for outputs) with SMR D1 = 0, D0 = 0.

| $T_A = -40^{\circ}\text{C to } 105^{\circ}\text{C}$ | | | | | | | |
|---|-----------|--|----------------------|-----|-----|-------|-------|
| 16 MHz | | | | | | | |
| No | Symbol | Parameter | Note [3] V_{CC} | Min | Max | Units | Notes |
| 1 | TdA(AS) | Address Valid to \overline{AS} Rise Delay | 4.5V | 25 | | ns | 2 |
| | | | 5.5V | 25 | | ns | |
| 2 | TdAS(A) | $\overline{AS}\overline{AS}$ Rise to Address Float Delay | 4.5V | 35 | | ns | 2 |
| | | | 5.5V | 35 | | ns | |
| 3 | TdAS(DR) | \overline{AS} Rise to Read Data Req'd Valid | 4.5V | | 180 | ns | 1,2 |
| | | | 5.5V | | 180 | ns | |
| 4 | TwAS | \overline{AS} Low Width | 4.5V | 40 | | ns | 2 |
| | | | 5.5V | 40 | | ns | |
| 5 | TdAS(DS) | Address Float to \overline{DS} Fall | 4.5V | 0 | | ns | |
| | | | 5.5V | 0 | | ns | |
| 6 | TwDSR | \overline{DS} (Read) Low Width | 4.5V | 135 | | ns | 1,2 |
| | | | 5.5V | 135 | | ns | |
| 7 | TwDSW | \overline{DS} (Write) Low Width | 4.5V | 80 | | ns | 1,2 |
| | | | 5.5V | 80 | | ns | |
| 8 | TdDSR(DR) | \overline{DS} Fall to Read Data Req'd Valid | 4.5V | | 75 | ns | 1,2 |
| | | | 5.5V | | 75 | ns | |
| 9 | ThDR(DS) | Read Data to \overline{DS} Rise Hold Time | 4.5V | 0 | | ns | 2 |
| | | | 5.5V | 0 | | ns | |
| 10 | TdDS(A) | \overline{DS} Rise to Address Active Delay | 4.5V | 50 | | ns | 2 |
| | | | 5.5V | 50 | | ns | |
| 11 | TdDS(AS) | \overline{DS} Rise to \overline{AS} Fall Delay | 4.5V | 35 | | ns | 2 |
| | | | 5.5V | 35 | | ns | |
| 12 | TdR/W(AS) | R/ \overline{W} Valid to \overline{AS} Rise Delay | 4.5V | 25 | | ns | 2 |
| | | | 5.5V | 25 | | ns | |
| 13 | TdDS(R/W) | \overline{DS} Rise to R/ \overline{W} Not Valid | 4.5V | 35 | | ns | 2 |
| | | | 5.5V | 35 | | ns | |
| 14 | TdDW(DSW) | Write Data Valid to \overline{DS} Fall (Write) Delay | 4.5V | 55 | 25 | ns | 2 |
| | | | 5.5V | 55 | 25 | ns | |
| 15 | TdDS(DW) | \overline{DS} Rise to Write Data Not Valid Delay | 4.5V | 35 | | ns | 2 |
| | | | 5.5V | 35 | | ns | |
| 16 | TdA(DR) | Address Valid to Read Data Req'd Valid | 4.5V | | 230 | ns | 1,2 |
| | | | 5.5V | | 230 | ns | |
| 17 | TdAS(DS) | \overline{AS} Rise to \overline{DS} Fall Delay | 4.5V | 45 | | ns | 2 |
| | | | 5.5V | 45 | | ns | |
| 18 | TdDM(AS) | /DM Valid to \overline{AS} Fall Delay | 4.5V | 30 | | ns | 2 |
| | | | 5.5V | 30 | | ns | |
| 20 | ThDS(AS) | \overline{DS} Valid to Address Valid Hold Time | 4.5V | 35 | | ns | |
| | | | 5.5V | 35 | | ns | |

Notes:

1. When using extended memory timing, add 2 TpC.
2. Timing numbers given are for minimum TpC.
3. The V_{CC} voltage specification of 5.5V guarantees 5.0V \pm 0.5V and the V_{CC} voltage specification of 3.5V guarantees only 3.5V

Standard Test Load

All timing references use 0.7 V_{CC} for a logic 1 and 0.2 V_{CC} for a logic 0.
For Standard Mode (not Low-EMI Mode for outputs) with SMR, D1 = 0, D0 = 0.

DC ELECTRICAL CHARACTERISTICS (Continued)

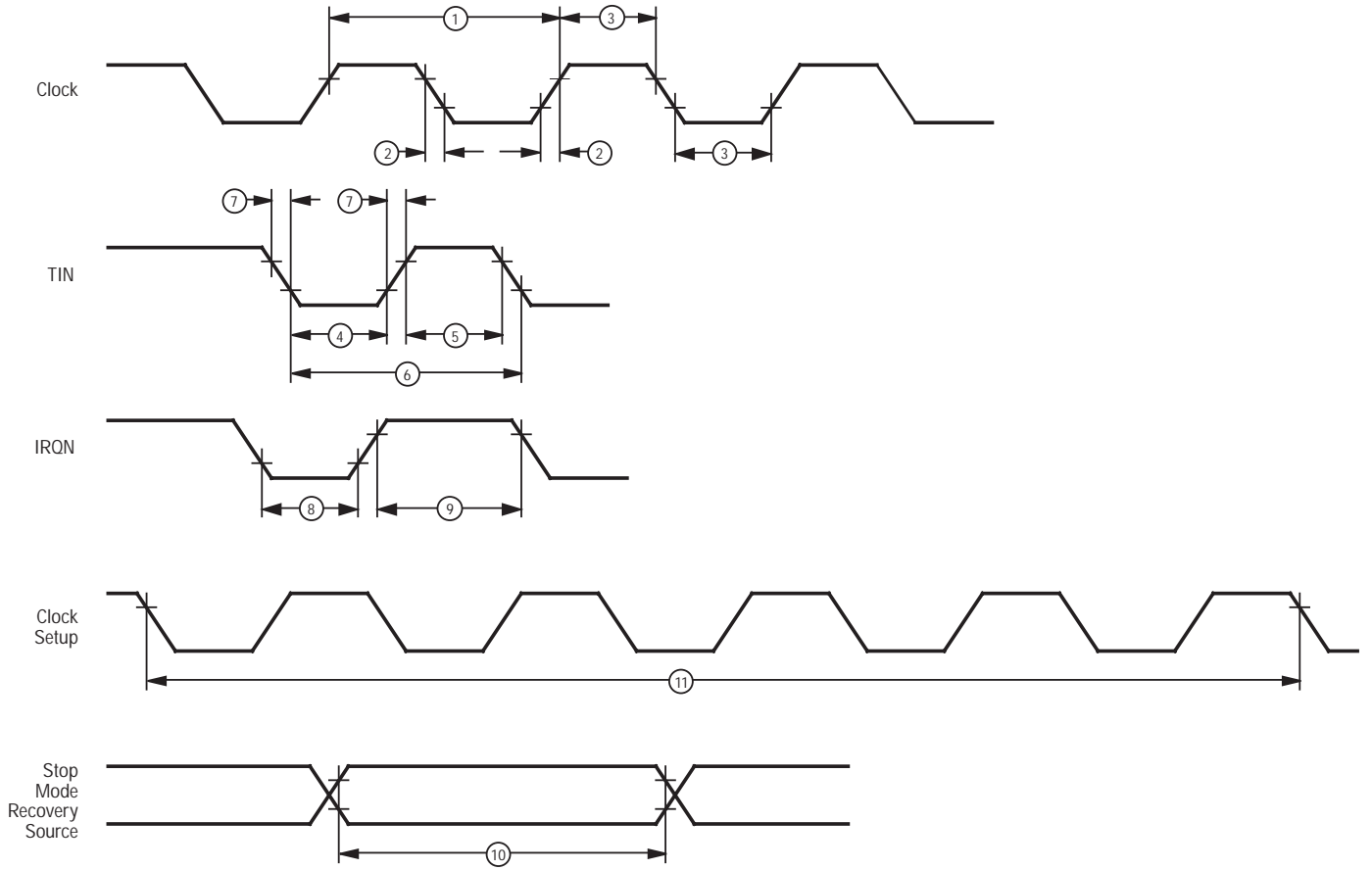


Figure 15. Additional Timing Diagram

Additional Timing Table (Divide-By-One Mode)

| No | Symbol | Parameter | V _{CC} Note [6] | T _A = 0 °C to +70 °C | | T _A = -40 °C to +105 °C | | Units | Notes |
|----|--------------|-------------------------------|-----------------------------|---------------------------------|------|------------------------------------|------|-------|---------|
| | | | | 4 MHz | | 4 MHz | | | |
| | | | | Min | Max | Min | Max | | |
| 1 | TpC | Input Clock Period | 3.5V | 250 | DC | 250 | DC | ns | 1,7,8 |
| | | | 5.5V | 250 | DC | 250 | DC | ns | 1,7,8 |
| 2 | TrC,TfC | Clock Input Rise & Fall Times | 3.5V | | 25 | | 25 | ns | 1,7,8 |
| | | | 5.5V | | 25 | | 25 | ns | 1,7,8 |
| 3 | TwC | Input Clock Width | 3.5V | 100 | | 100 | | ns | 1,7,8 |
| | | | 5.5V | 100 | | 100 | | ns | 1,7,8 |
| 4 | TwTinL | Timer Input Low Width | 3.5V | 100 | | 100 | | ns | 1,7,8 |
| | | | 5.5V | 70 | | 70 | | ns | 1,7,8 |
| 5 | TwTinH | Timer Input High Width | 3.5V | 5TpC | | 5TpC | | | 1,7,8 |
| | | | 5.5V | 5TpC | | 5TpC | | | 1,7,8 |
| 6 | TpTin | Timer Input Period | 3.5V | 8TpC | | 8TpC | | | 1,7,8 |
| | | | 5.5V | 8TpC | | 8TpC | | | 1,7,8 |
| 7 | TrTin, Tftin | Timer Input Rise & Fall Timer | 3.5V | | 100 | | 100 | ns | 1,7,8 |
| | | | 5.5V | | 100 | | 100 | ns | 1,7,8 |
| 8A | TwIL | Int. Request Low Time | 3.5V | 100 | | 100 | | ns | 1,2,7,8 |
| | | | 5.5V | 70 | | 70 | | ns | 1,2,7,8 |
| 8B | TwIL | Int. Request Low Time | 3.5V | 5TpC | | 5TpC | | | 1,3,7,8 |
| | | | 5.5V | 5TpC | | 5TpC | | | 1,3,7,8 |
| 9 | TwiH | Int. Request Input High Time | 3.5V | 5TpC | | 5TpC | | | 1,2,7,8 |
| | | | 5.5V | 5TpC | | 5TpC | | | 1,2,7,8 |
| 10 | Twsm | STOP Mode | 3.5V | 12 | | 12 | | ns | 4,8 |
| | | Recovery Width Spec | 5.5V | 12 | | 12 | | ns | 4,8 |
| 11 | Tost | Oscillator Startup Time | 3.5V | | 5TpC | | 5TpC | | 4,8,9 |
| | | | 5.5V | | 5TpC | | 5TpC | | 4,8,9 |

Notes:

- Timing Reference uses 0.7 V_{CC} for a logic 1 and 0.2 V_{CC} for a logic 0.
- Interrupt request via Port 3 (P31–P33).
- Interrupt request via Port 3 (P30).
- SMR-D5 = 1, POR STOP Mode Delay is on.
- Reg. WDTMR.
- The V_{CC} voltage specification of 5.5V guarantees 5.0V ± 0.5V and the V_{CC} voltage specification of 3.5V guarantees 3.5V only.
- SMR D1 = 0.
- Maximum frequency for internal system clock is 4 MHz when using XTAL divide-by-one mode.
- For RC and LC oscillator, and for oscillator driven by clock driver.

DC ELECTRICAL CHARACTERISTICS (Continued)

Handshake Timing Diagrams



Figure 16. Input Handshake Timing



Figure 17. Output Handshake Timing

Additional Timing Table

| $T_A = -40\text{ }^\circ\text{C to } +105\text{ }^\circ\text{C}$ | | | | | | | | |
|--|--------------|---|----------------------|------|------|-------|------------|---------|
| 16 MHz | | | | | | | | |
| No | Symbol | Parameter | V_{CC} Note [6] | Min | Max | Units | Conditions | Notes |
| 1 | TpC | Input Clock Period | 3.5V | 62.5 | DC | ns | | 1,7,8 |
| | | | 5.5V | 62.5 | DC | ns | | 1,7,8 |
| 2 | TrC,TfC | Clock Input Rise & Fall Times | 3.5V | | 15 | ns | | 1,7,8 |
| | | | 5.5V | | 15 | ns | | 1,7,8 |
| 3 | TwC | Input Clock Width | 3.5V | 31 | | ns | | 1,7,8 |
| | | | 5.5V | 31 | | ns | | 1,7,8 |
| 4 | TwTinL | Timer Input Low Width | 3.5V | 70 | | ns | | 1,7,8 |
| | | | 5.5V | 70 | | ns | | 1,7,8 |
| 5 | TwTinH | Timer Input High Width | 3.5V | 5TpC | | | | 1,7,8 |
| | | | 5.5V | 5TpC | | | | 1,7,8 |
| 6 | TpTin | Timer Input Period | 3.5V | 8TpC | | | | 1,7,8 |
| | | | 5.5V | 8TpC | | | | 1,7,8 |
| 7 | TrTin, TfTin | Timer Input Rise & Fall Timer | 3.5V | | 100 | ns | | 1,7,8 |
| | | | 5.5V | | 100 | ns | | 1,7,8 |
| 8A | TwlL | Int. Request Low Time | 3.5V | 70 | | ns | | 1,2,7,8 |
| | | | 5.5V | 70 | | ns | | 1,2,7,8 |
| 8B | TwlL | Int. Request Low Time | 3.5V | 5TpC | | | | 1,3,7,8 |
| | | | 5.5V | 5TpC | | | | 1,3,7,8 |
| 9 | TwlH | Int. Request Input High Time | 3.5V | 5TpC | | | | 1,2,7,8 |
| | | | 5.5V | | | | | |
| 10 | Twsm | STOP Mode | 3.5V | 12 | | ns | | 4,8 |
| | | Recovery Width Spec | 5.5V | 12 | | ns | | 4,8 |
| 11 | Tost | Oscillator Startup Time | 3.5V | | 5TpC | | | 4,8 |
| | | | 5.5V | | 5TpC | | | 4,8 |
| 12 | Twdt | Watch-Dog Timer Delay Time Before Timeout | 3.5V | 10 | | ms | D0 = 0 | 5,11 |
| | | | 5.5V | 5 | | ms | D1 = 0 | 5,11 |
| | | | 3.5V | 20 | | ms | D0 = 1 | 5,11 |
| | | | 5.5V | 10 | | ms | D1 = 0 | 5,11 |
| | | | 3.5V | 40 | | ms | D0 = 0 | 5,11 |
| | | | 5.5V | 20 | | ms | D1 = 1 | 5,11 |
| | | | 3.5V | 160 | | ms | D0 = 1 | 5,11 |
| | | | 5.5V | 80 | | ms | D1 = 1 | 5,11 |

Notes:

- Timing Reference uses 0.7 V_{CC} for a logic 1 and 0.2 V_{CC} for a logic 0.
- Interrupt request via Port 3 (P31–P33)
- Interrupt request via Port 3 (P30)
- SMR-D5 = 1, POR STOP Mode Delay is on
- Reg. WDTMR
- The V_{CC} voltage spec. of 5.5V guarantees 5.0V \pm 0.5V.
- SMR D1 = 0
- Maximum frequency for internal system clock is 4 MHz when using XTAL divide-by-one mode.
- For RC and LC oscillator, and for oscillator driven by clock driver.
- Standard Mode (not Low EMI output ports)
- Using internal RC

PIN FUNCTIONS

EPROM Programming Mode

D7–D0 Data Bus. The data can be read from or written to external memory through the data bus.

A11–A0 Address Bus. During programming, the EPROM address is written to the address bus.

V_{CC} Power Supply. This pin must supply 5V during the EPROM read mode and 6V during other modes.

\overline{CE} Chip Enable (active Low). This pin is active during EPROM Read Mode, Program Mode, and Program Verify Mode.

\overline{OE} Output Enable (active Low). This pin drives the direction of the Data Bus. When this pin is Low, the Data Bus is output, when High, the Data Bus is input.

EPM EPROM Program Mode. This pin controls the different EPROM Program Mode by applying different voltages.

V_{PP} Program Voltage. This pin supplies the program voltage.

\overline{PGM} Program Mode (active Low). When this pin is Low, the data is programmed to the EPROM through the Data Bus.

Application Precaution

The production test-mode environment may be enabled accidentally during normal operation if excessive noise surges above V_{CC} occur on pins XTAL1 and \overline{RESET} .

In addition, processor operation of Z8 OTP devices may be affected by excessive noise surges on the V_{PP} , \overline{CE} , \overline{EPM} , \overline{OE} pins while the microcontroller is in Standard Mode.

Recommendations for dampening voltage surges in both test and OTP mode include the following:

- Using a clamping diode to V_{CC}
- Adding a capacitor to the affected pin

Standard Mode

XTAL Crystal 1 (time-based input). This pin connects a parallel-resonant crystal, ceramic resonator, LC, RC network, or external single-phase clock to the on-chip oscillator input.

XTAL2 Crystal 2 (time-based output). This pin connects a parallel-resonant crystal, ceramic resonator, LC, or RC network to the on-chip oscillator output.

R/\overline{W} Read/Write (output, write Low). The R/\overline{W} signal is Low when the CCP is writing to the external program or data memory (Z86E40 only).

\overline{RESET} Reset (input, active Low). Reset will initialize the MCU. Reset is accomplished either through Power-On, Watch-Dog Timer reset, STOP-Mode Recovery, or external reset. During Power-On Reset and Watch-Dog Timer Reset, the internally generated reset drives the reset pin low for the POR time. Any devices driving the reset line must be open-drain in order to avoid damage from a possible conflict during reset conditions. Pull-up is provided internally. After the POR time, \overline{RESET} is a Schmitt-triggered input.

To avoid asynchronous and noisy reset problems, the Z86E40 is equipped with a reset filter of four external clocks (4TpC). If the external reset signal is less than 4TpC in duration, no reset occurs. On the fifth clock after the reset is detected, an internal RST signal is latched and held for an internal register count of 18 external clocks, or for the duration of the external reset, whichever is longer. During the reset cycle, \overline{DS} is held active Low while \overline{AS} cycles at a rate of TpC/2. Program execution begins at location 000CH, 5–10 TpC cycles after \overline{RESET} is released. For Power-On Reset, the reset output time is 5 ms. The Z86E40 does not reset WDTMR, SMR, P2M, and P3M registers on a STOP-Mode Recovery operation.

$\overline{ROMless}$ (input, active Low). This pin, when connected to GND, disables the internal ROM and forces the device to function as a Z86C90/C89 ROMless Z8. (Note that, when left unconnected or pulled High to V_{CC} , the device functions normally as a Z8 ROM version).

Note: When using in ROM Mode in High EMI (noisy) environment, the ROMless pins should be connected directly to V_{CC} .

Port 0 (P07–P00). Port 0 is an 8-bit, bidirectional, CMOS-compatible I/O port. These eight I/O lines can be configured under software control as a nibble I/O port, or as an address port for interfacing external memory. The input buffers are Schmitt-triggered and nibble programmed. Either nibble output that can be globally programmed as push-pull or open-drain. Low EMI output buffers can be globally programmed by the software. Port 0 can be placed under handshake control. In Handshake Mode, Port 3 lines P32 and P35 are used as handshake control lines. The handshake direction is determined by the configuration (input or output) assigned to Port 0's upper nibble. The lower nibble must have the same direction as the upper nibble.

For external memory references, Port 0 provides address bits A11–A8 (lower nibble) or A15–A8 (lower and upper

nibble) depending on the required address space. If the address range requires 12 bits or less, the upper nibble of Port 0 can be programmed independently as I/O while the lower nibble is used for addressing. If one or both nibbles are needed for I/O operation, they must be configured by writing to the Port 0 mode register. In ROMless mode, after a hardware reset, Port 0 is configured as address lines A15–A8, and extended timing is set to accommodate slow memory access. The initialization routine can include re-configuration to eliminate this extended timing mode. In ROM mode, Port 0 is defined as input after reset.

Port 0 can be set in the High-Impedance Mode if selected as an address output state, along with Port 1 and the control signals \overline{AS} , \overline{DS} , and R/\overline{W} (Figure 18).

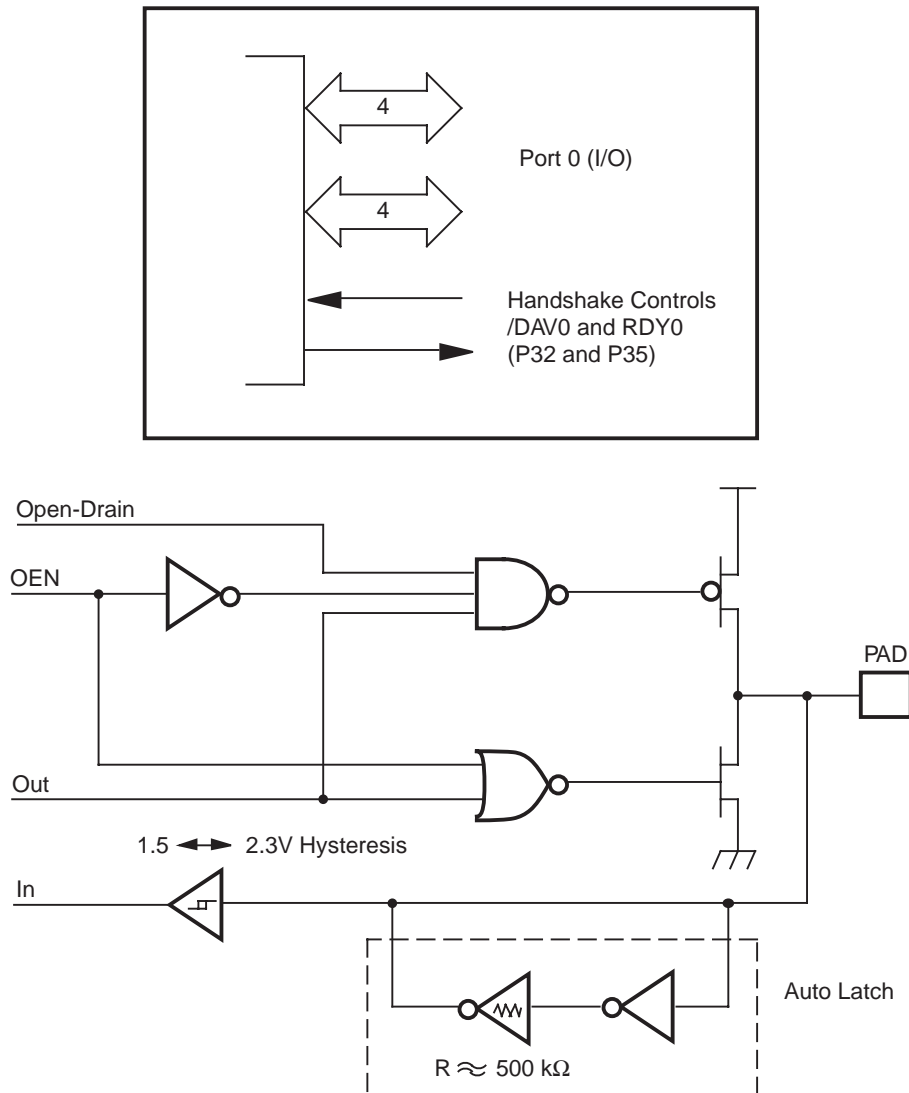


Figure 18. Port 0 Configuration

PIN FUNCTIONS (Continued)

Port 1 (P17–P10). Port 1 is an 8-bit, bidirectional, CMOS-compatible port with multiplexed Address (A7–A0) and Data (D7–D0) ports. These eight I/O lines can be programmed as inputs or outputs or can be configured under software control as an Address/Data port for interfacing external memory. The input buffers are Schmitt-triggered and the output buffers can be globally programmed as either push-pull or open-drain. Low EMI output buffers can be globally programmed by the software. Port 1 can be placed under handshake control. In this configuration, Port 3, lines P33 and P34 are used as the handshake controls

RDY1 and /DAV1 (Ready and Data Available). To interface external memory, Port 1 must be programmed for the multiplexed Address/Data mode. If more than 256 external locations are required, Port 0 outputs the additional lines (Figure 19).

Port 1 can be placed in the high-impedance state along with Port 0, \overline{AS} , \overline{DS} , and R/\overline{W} , allowing the Z86E40 to share common resources in multiprocessor and DMA applications.

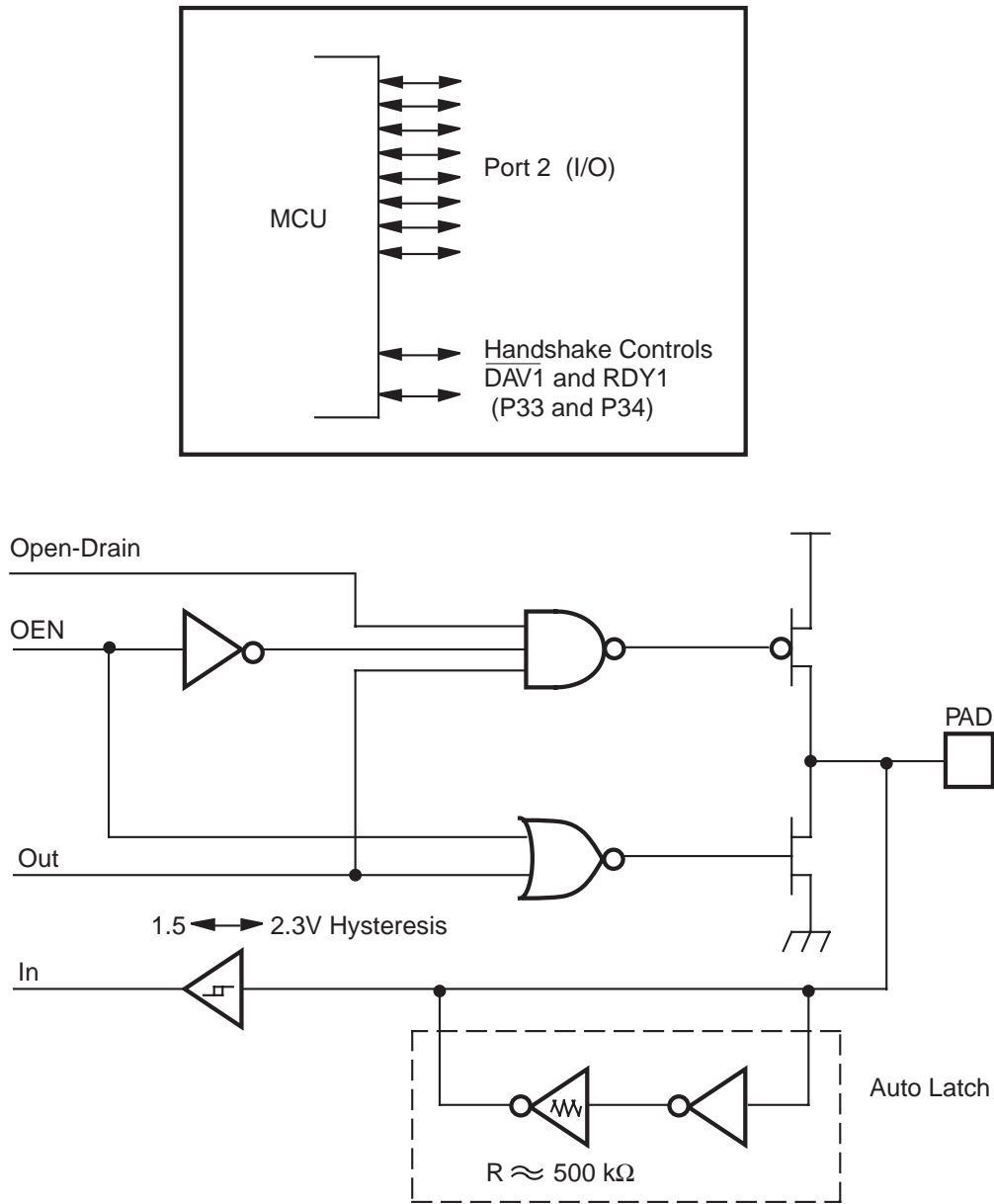


Figure 19. Port 1 Configuration (Z86E40 Only)

Port 2 (P27–P20). Port 2 is an 8-bit, bidirectional, CMOS-compatible I/O port. These eight I/O lines can be configured under software control as an input or output, independently. All input buffers are Schmitt-triggered. Bits programmed as outputs can be globally programmed as either push-pull or open-drain. Low EMI output buffers can

be globally programmed by the software. When used as an I/O port, Port 2 can be placed under handshake control.

In Handshake Mode, Port 3 lines P31 and P36 are used as handshake control lines. The handshake direction is determined by the configuration (input or output) assigned to bit 7 of Port 2 (Figure 20).

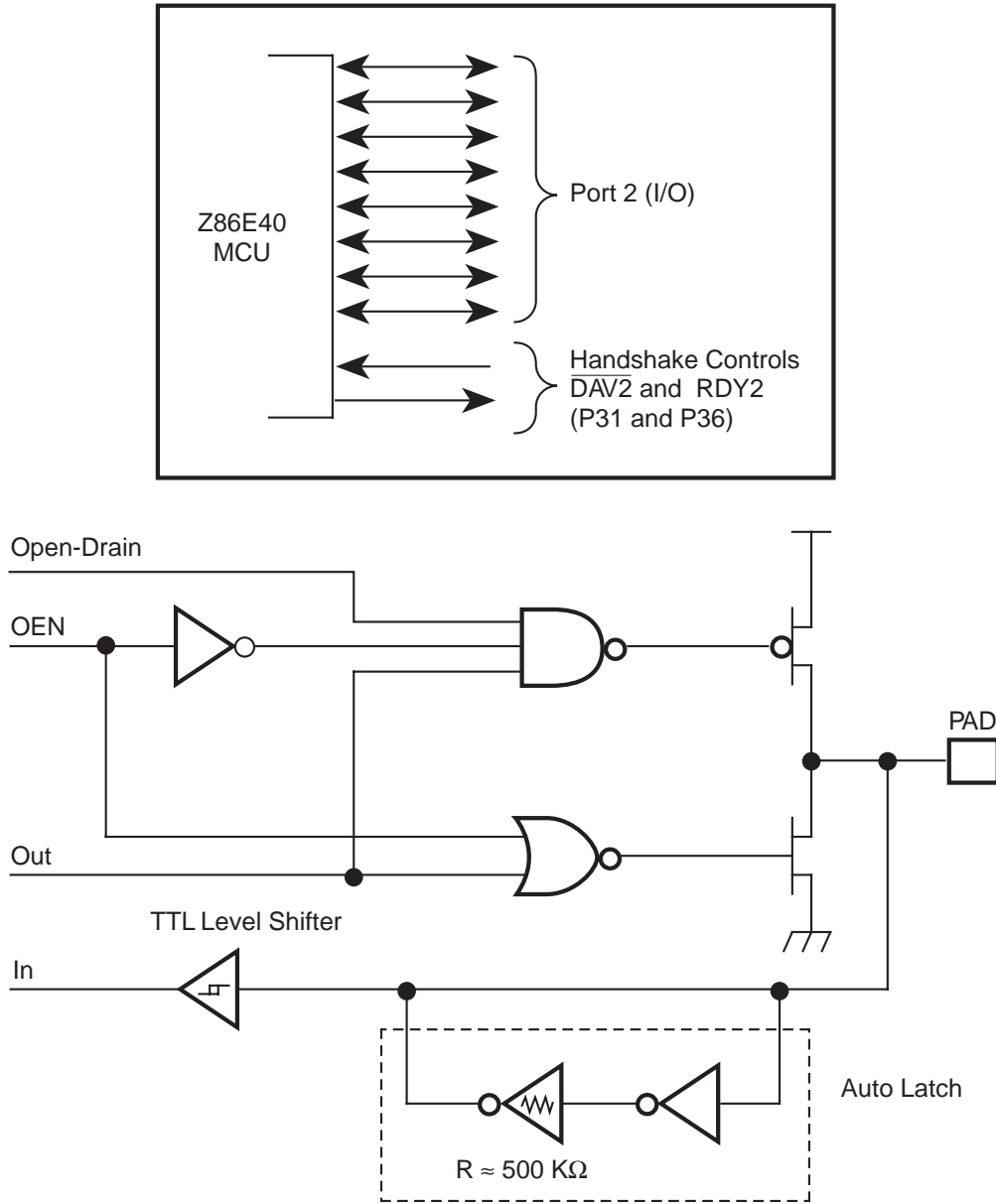


Figure 20. Port 2 Configuration

PIN FUNCTIONS (Continued)

Port 3 (P37–P30). Port 3 is an 8-bit, CMOS-compatible port with four fixed inputs (P33–P30) and four fixed outputs (P37–P34). These eight lines can be configured by software for interrupt and handshake control functions. Port 3, Pin 0 is Schmitt-triggered. P31, P32, and P33 are standard CMOS inputs with single trip point (no Auto Latches) and P34, P35, P36, and P37 are push-pull output lines. Low EMI output buffers can be globally programmed by the software. Two on-board comparators can process analog signals on P31 and P32 with reference to the voltage on P33. The analog function is enabled by setting the D1 of Port 3 Mode Register (P3M). The comparator output can be outputted from P34 and P37, respectively, by setting PCON register Bit D0 to 1 state. For the interrupt function, P30 and P33 are falling edge triggered interrupt inputs. P31 and P32 can be programmed as falling, rising or both edges triggered interrupt inputs (Figure 21). Access to Counter/Timer 1 is made through P31 (T_{IN}) and P36 (T_{OUT}). Handshake lines for Port 0, Port 1, and Port 2 are also available on Port 3 (Table 9).

Note: When enabling/ or disabling analog mode, the following is recommended:

1. Allow two NOP delays before reading this comparator output.
2. Disable global interrupts, switch to analog mode, clear interrupts, and then re-enable interrupts.
3. IRQ register bits 3 to 0 must be cleared after enabling analog mode.

Note: P33–P30 differs from the Z86C30/C31/C40 in that there is no clamping diode to V_{CC} due to the EPROM high-voltage circuits. Exceeding the V_{IH} maximum specification during standard operating mode may cause the device to enter EPROM mode.

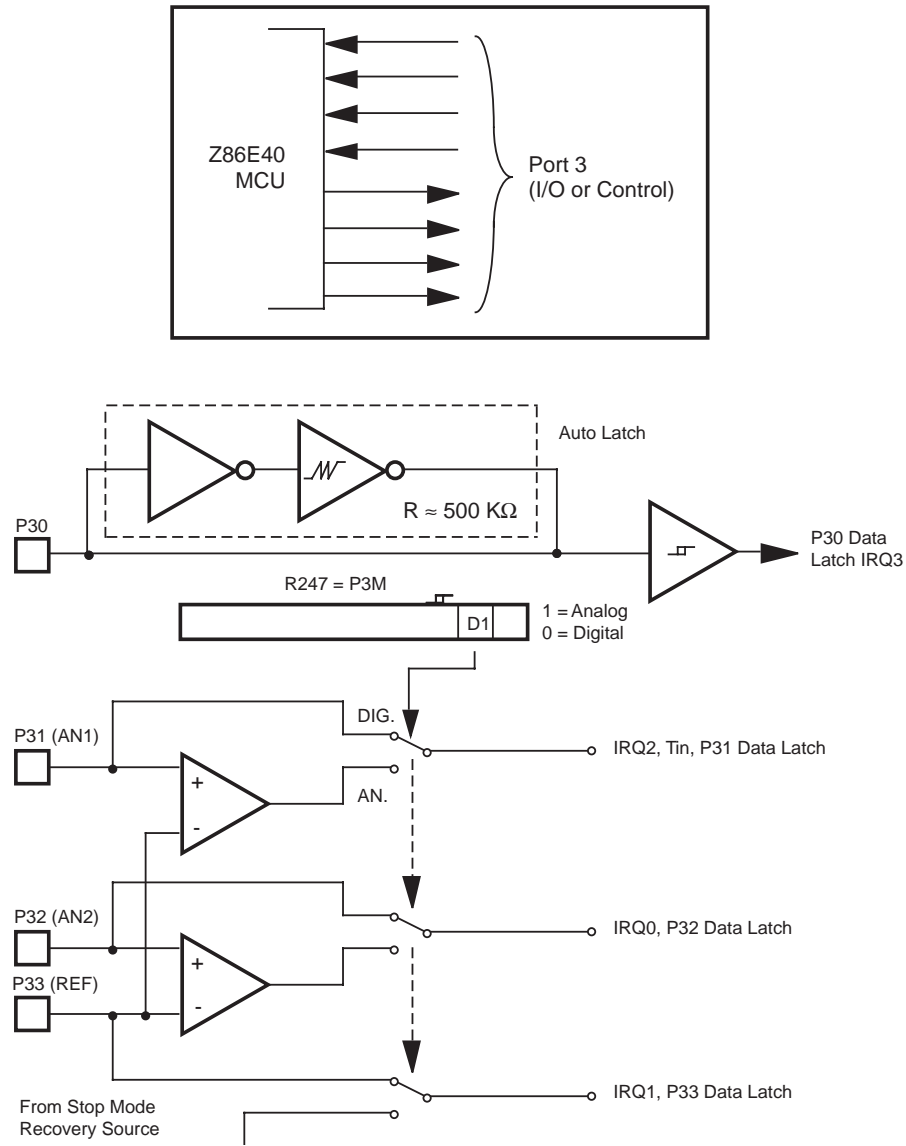


Figure 21. Port 3 Configuration

Table 9. Port 3 Pin Assignments

| Pin | I/O | CTC1 | Analog | Interrupt | P0 HS | P1 HS | P2 HS | Ext |
|-----|-----|------------------|---------|-----------|-------|-------|-------|-----|
| P30 | IN | | | IRQ3 | | | | |
| P31 | IN | T _{IN} | AN1 | IRQ2 | | D/R | | |
| P32 | IN | | AN2 | IRQ0 | D/R | | | |
| P33 | IN | | REF | IRQ1 | | D/R | | |
| P34 | OUT | | AN1-Out | | | R/D | | /DM |
| P35 | OUT | | | | R/D | | | |
| P36 | OUT | T _{OUT} | | | | R/D | | |
| P37 | OUT | | An2-Out | | | | | |

PIN FUNCTIONS (Continued)

Comparator Inputs. Port 3, P31, and P32, each have a comparator front end. The comparator reference voltage P33 is common to both comparators. In analog mode, P31 and P32 are the positive input of the comparators and P33 is the reference voltage of the comparators.

Auto Latch. The Auto Latch puts valid CMOS levels on all CMOS inputs (except P33–P31) that are not externally driven. Whether this level is 0 or 1, cannot be determined. A valid CMOS level, rather than a floating node, reduces excessive supply current flow in the input buffer. Auto Latches are available on Port 0, Port 2, and P30. There are no Auto Latches on P31, P32, and P33.

Low EMI Emission. The Z86E40 can be programmed to operate in a low EMI Emission Mode in the PCON register. The oscillator and all I/O ports can be programmed as low EMI emission mode independently. Use of this feature results in:

- The pre-drivers slew rate reduced to 10 ns typical.
- Low EMI output drivers have resistance of 200 Ohms (typical).
- Low EMI Oscillator.
- Internal SCLK/TCLK= XTAL operation limited to a maximum of 4 MHz – 250 ns cycle time, when Low EMI Oscillator is selected and system clock (SCLK = XTAL, SMR Reg. Bit D1 =1).
- **Note for emulation only:**
Do not set the emulator to emulate Port 1 in low EMI mode. Port 1 must always be configured in Standard Mode.

FUNCTIONAL DESCRIPTION

The MCU incorporates the following special functions to enhance the standard Z8 architecture to provide the user with increased design flexibility.

RESET. The device is reset in one of three ways:

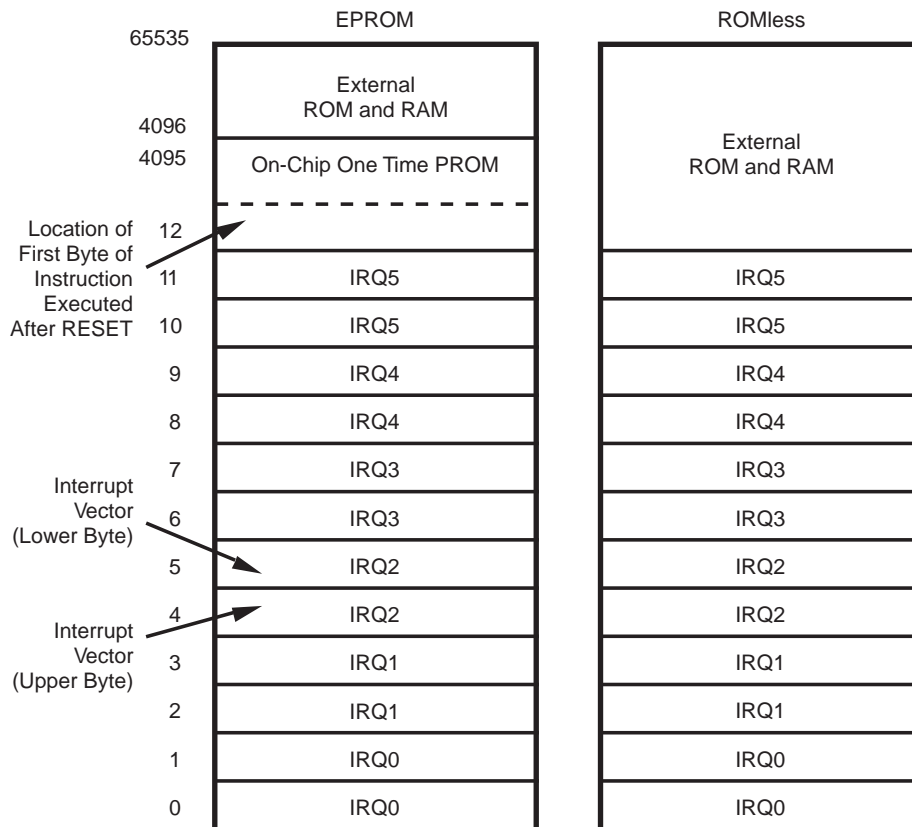
1. Power-On Reset
2. Watch-Dog Timer
3. STOP-Mode Recovery Source

Note: Having the Auto Power-On Reset circuitry built-in, the MCU does not need to be connected to an external power-on reset circuit. The reset time is 5 ms (typical). The MCU does not reinitialize WDTMR, SMR, P2M, and P3M registers to their reset values on a STOP-Mode Recovery operation.

Note: The device V_{CC} must rise up to the operating V_{CC} specification before the TPOR expires.

Program Memory. The MCU can address up to 4 KB of Internal Program Memory (Figure 22). The first 12 bytes of program memory are reserved for the interrupt vectors. These locations contain six 16-bit vectors that correspond to the six available interrupts. For EPROM mode, byte 12 (000CH) to address 4095 (0FFFH) consists of program-mable EPROM. After reset, the program counter points at the address 000CH, which is the starting address of the user program.

In ROMless mode, the Z86E40 can address up to 64 KB of External Program Memory. The ROM/ROMless option is only available on the 44-pin devices.



**Figure 22. Program Memory Map
(ROMless Z86E40 Only)**

EPROM Protect. When in ROM Protect Mode, and executing out of External Program Memory, instructions LDC, LDCI, LDE, and LDEI cannot read Internal Program Memory.

When in ROM Protect Mode and executing out of Internal Program Memory, instructions LDC, LDCI, LDE, and LDEI can read Internal Program Memory.

FUNCTIONAL DESCRIPTION (Continued)

Data Memory (\overline{DM}). In EPROM Mode, the Z86E40 can address up to 60 KB of external data memory beginning at location 4096. In ROMless mode, the Z86E40 can address up to 64 KB of data memory. External data memory may be included with, or separated from, the external program memory space. \overline{DM} , an optional I/O function that can be

programmed to appear on pin P34, is used to distinguish between data and program memory space (Figure 23). The state of the \overline{DM} signal is controlled by the type of instruction being executed. An LDC opcode references PROGRAM (\overline{DM} inactive) memory, and an LDE instruction references data (\overline{DM} active Low) memory.

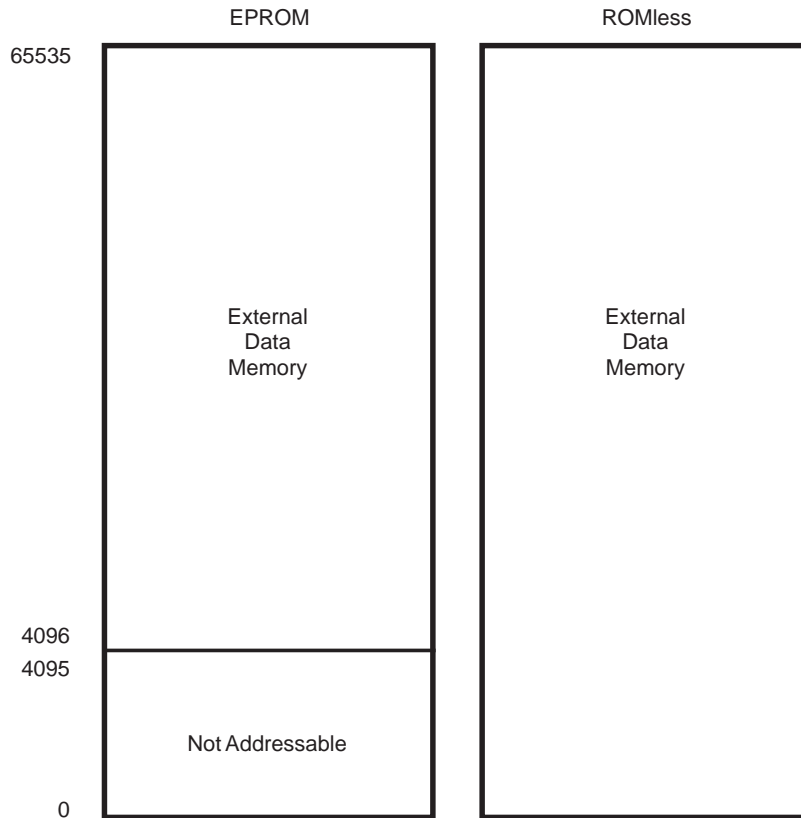


Figure 23. Data Memory Map

Register File. The register file consists of three I/O port registers, 236/125 general-purpose registers, 15 control and status registers, and three system configuration registers in the expanded register group. The instructions can access registers directly or indirectly through an 8-bit address field. This allows a short 4-bit register address using the Register Pointer (Figure 24). In the 4-bit mode, the register file is divided into 16 working register groups, each

occupying 16 continuous locations. The Register Pointer addresses the starting location of the active working-register group.

Note: Register Bank E0–EF can only be accessed through working register and indirect addressing modes. (This bank is available in Z86E30/E40 only.)



Figure 24. Register Pointer Register

Expanded Register File (ERF). The register file has been expanded to allow for additional system control registers, mapping of additional peripheral devices and input/output ports into the register address area. The Z8 register address space R0 through R15 is implemented as 16 groups of 16 registers per group (Figure 26). These register groups are known as the Expanded Register File (ERF).

The low nibble (D3–D0) of the Register Pointer (RP) select the active ERF group, and the high nibble (D7–D4) of register RP select the working register group. Three system configuration registers reside in the Expanded Register File at bank FH: PCON, SMR, and WDTMR. The rest of the Expanded Register is not physically implemented and is reserved for future expansion.

FUNCTIONAL DESCRIPTION (Continued)



Figure 25. Register Pointer

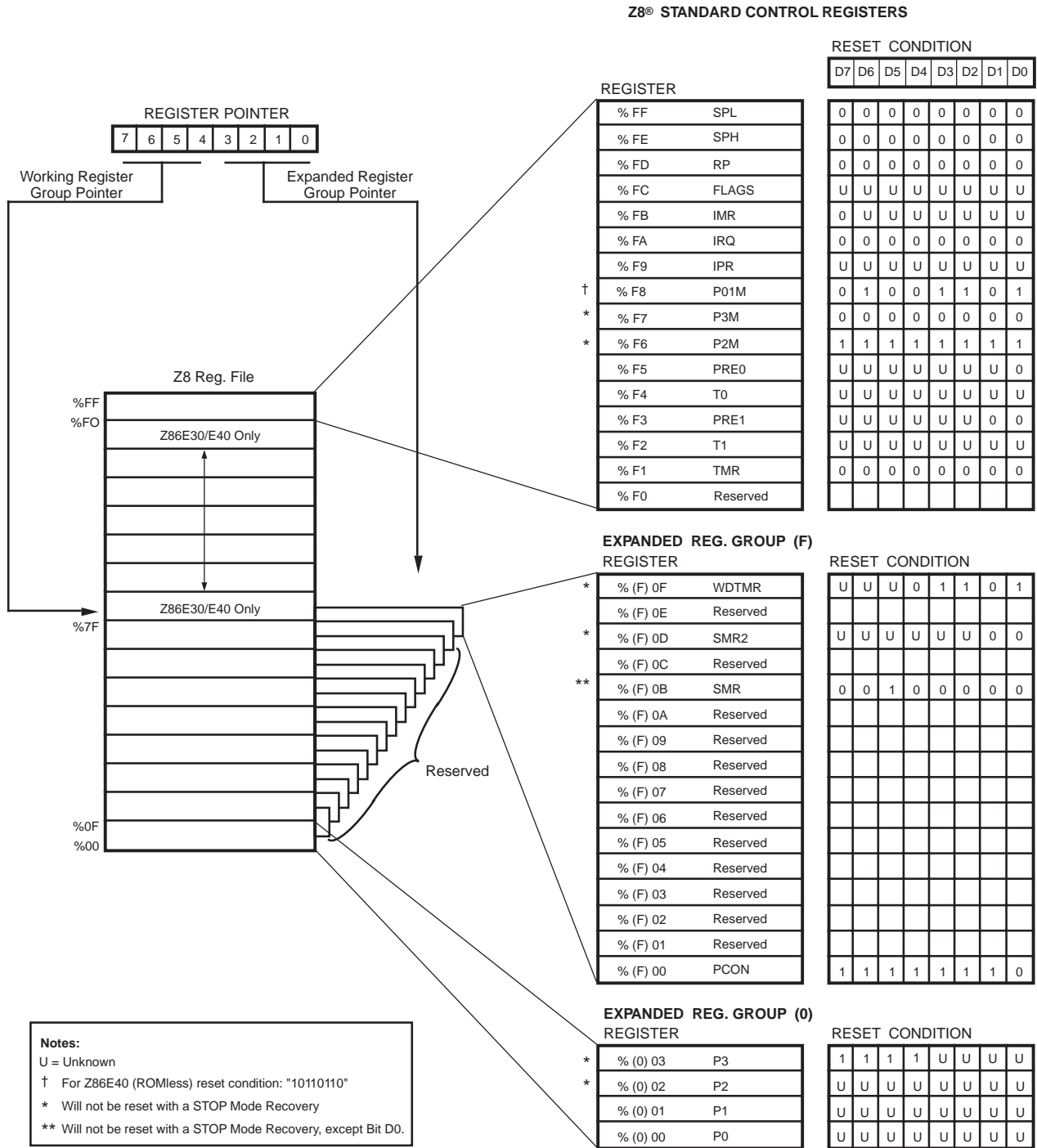


Figure 26. Expanded Register File Architecture

FUNCTIONAL DESCRIPTION (Continued)

General-Purpose Registers (GPR). These registers are undefined after the device is powered up. The registers keep their last value after any reset, as long as the reset occurs in the V_{CC} voltage-specified operating range. The register R254 is general-purpose on Z86E30/E31. R254 and R255 are set to 00H after any reset or STOP-Mode Recovery.

RAM Protect. The upper portion of the RAM's address spaces 80H to EFH (excluding the control registers) can be protected from reading and writing. This option can be selected during the EPROM Programming Mode. After this option is selected, the user can activate this feature from the internal EPROM. D6 of the IMR control register (R251) is used to turn off/on the RAM protect by loading a 0 or 1, respectively. A "1" in D6 indicates RAM Protect enabled. RAM Protect is not available on the Z86E31.

Stack. The Z86E40 external data memory or the internal register file can be used for the stack. The 16-bit Stack Pointer (R254–R255) is used for the external stack, which can reside anywhere in the data memory for ROMless mode, but only from 4096 to 65535 in ROM mode. An 8-bit Stack Pointer (R255) is used for the internal stack on the Z86E30/E31/E40 that resides within the 236 general-purpose registers (R4–R239). SPH (R254) can be used as a general-purpose register when using internal stack only. R254 and R255 are set to 00H after any reset or Stop-Mode Recovery.

Counter/Timers. There are two 8-bit programmable counter/timers (T0 and T1), each driven by its own 6-bit programmable prescaler. The T1 prescaler is driven by internal or external clock sources; however, the T0 prescaler is driven by the internal clock only (Figure 27).

The 6-bit prescalers can divide the input frequency of the clock source by any integer number from 1 to 64. Each prescaler drives its counter, which decrements the value (1 to 256), that has been loaded into the counter. When the counter reaches the end of count, a timer interrupt request, IRQ4 (T0) or IRQ5 (T1), is generated.

The counters can be programmed to start, stop, restart to continue, or restart from the initial value. The counters can also be programmed to stop upon reaching zero (single pass mode) or to automatically reload the initial value and continue counting (modulo-n continuous mode).

The counters, but not the prescalers, can be read at any time without disturbing their value or count mode. The clock source for T1 is user-definable and can be either the internal microprocessor clock divided by four, or an external signal input through Port 3. The Timer Mode register configures the external timer input (P31) as an external clock, a trigger input that can be retriggerable or non-retriggerable, or as a gate input for the internal clock. Port 3 line P36 serves as a timer output (T_{OUT}) through which T0, T1, or the internal clock can be output. The counter/timers can be cascaded by connecting the T0 output to the input of T1.



Figure 27. Counter/Timer Block Diagram

FUNCTIONAL DESCRIPTION (Continued)

Interrupts. The MCU has six different interrupts from six different sources. The interrupts are maskable and prioritized (Figure 28). The six sources are divided as follows: four sources are claimed by Port 3 lines P33–P30) and two

in counter/timers. The Interrupt Mask Register globally or individually enables or disables the six interrupt requests (Table 10).



Figure 28. Interrupt Block Diagram

Table 10. Interrupt Types, Sources, and Vectors

| Name | Source | Vector Location | Comments |
|------|---|-----------------|---|
| IRQ0 | $\overline{DAV0}$, IRQ0 | 0, 1 | External (P32), Rising/Falling Edge Triggered |
| IRQ1 | IRQ1 | 2, 3 | External (P33), Falling Edge Triggered |
| IRQ2 | $\overline{DAV2}$, IRQ2, T _{IN} | 4, 5 | External (P31), Rising/Falling Edge Triggered |
| IRQ3 | IRQ3 | 6, 7 | External (P30), Falling Edge Triggered |
| IRQ4 | T0 | 8, 9 | Internal |
| IRQ5 | T1 | 10, 11 | Internal |

When more than one interrupt is pending, priorities are resolved by a programmable priority encoder that is controlled by the Interrupt Priority Register (IPR). An interrupt machine cycle is activated when an interrupt request is granted. Thus, disabling all subsequent interrupts, saves the Program Counter and Status Flags, and then branches to the program memory vector location reserved for that interrupt. All interrupts are vectored through locations in the program memory. This memory location and the next byte contain the 16-bit starting address of the interrupt service routine for that particular interrupt request.

To accommodate polled interrupt systems, interrupt inputs are masked and the interrupt request register is polled to determine which of the interrupt requests need service.

An interrupt resulting from AN1 is mapped into IRQ2, and an interrupt from AN2 is mapped into IRQ0. Interrupts IRQ2 and IRQ0 may be rising, falling or both edge triggered, and are programmable by the user. The software may poll to identify the state of the pin.

Programming bits for the Interrupt Edge Select are located in bits D7 and D6 of the IRQ Register (R250). The configuration is shown in Table 11.

Table 11. IRQ Register Configuration

| IRQ | | Interrupt Edge | |
|-----|----|----------------|-----|
| D7 | D6 | P31 | P32 |
| 0 | 0 | F | F |
| 0 | 1 | F | R |
| 1 | 0 | R | F |
| 1 | 1 | R/F | R/F |

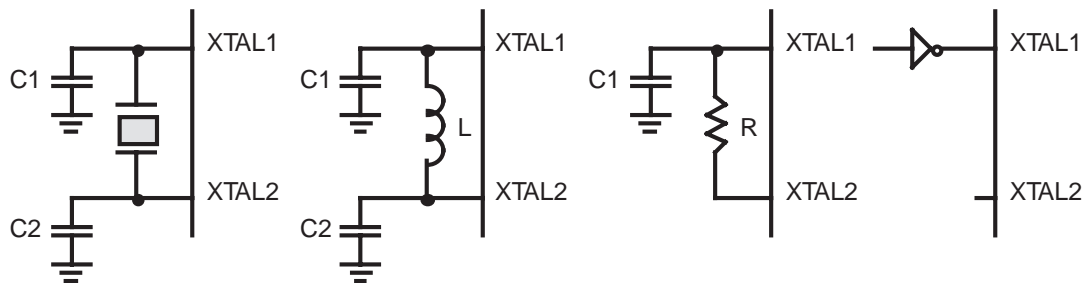
Notes:

F = Falling Edge

R = Rising Edge

Clock. The on-chip oscillator has a high-gain, parallel-resonant amplifier for connection to a crystal, RC, ceramic resonator, or any suitable external clock source (XTAL1 = Input, XTAL2 = Output). The crystal should be AT cut, 10 KHz to 16 MHz max, with a series resistance (RS) less than or equal to 100 Ohms.

The crystal should be connected across XTAL1 and XTAL2 using the vendor's recommended capacitor values from each pin directly to device pin Ground. The RC oscillator option can be selected in the programming mode. The RC oscillator configuration must be an external resistor connected from XTAL1 to XTAL2, with a frequency-setting capacitor from XTAL1 to Ground (Figure 29).



Ceramic Resonator or
Crystal
C1, C2 = 47 pF TYP *
F = 8 MHz

LC
C1, C2 = 22 pF
L = 130 μ H *
F = 3 MHz *

RC
@ 5V V_{CC} (TYP)
C1 = 100 pF
R = 2K
F = 6 MHz

External Clock

* Typical value including pin parasitics

Figure 29. Oscillator Configuration

FUNCTIONAL DESCRIPTION (Continued)

Power-On Reset (POR). A timer circuit clocked by a dedicated on-board RC oscillator is used for the Power-On Reset (POR) timer function. The POR timer allows V_{CC} and the oscillator circuit to stabilize before instruction execution begins.

The POR timer circuit is a one-shot timer triggered by one of three conditions:

1. Power fail to Power OK status
2. Stop-Mode Recovery (if D5 of SMR=0)
3. WDT time-out

The POR time is a nominal 5 ms. Bit 5 of the STOP mode Register (SMR) determines whether the POR timer is bypassed after STOP-Mode Recovery (typical for an external clock and RC/LC oscillators with fast start up times).

HALT. Turns off the internal CPU clock, but not the XTAL oscillation. The counter/timers and external interrupt IRQ0, IRQ1, and IRQ2 remain active. The device is recovered by interrupts, either externally or internally generated. An interrupt request must be executed (enabled) to exit HALT Mode. After the interrupt service routine, the program continues from the instruction after the HALT.

In order to enter STOP or HALT Mode, it is necessary to first flush the instruction pipeline to avoid suspending execution in mid-instruction. To do this, the user must execute a NOP (Opcode=FFH) immediately before the appropriate sleep instruction, that is:

| | | |
|----|------|----------------------|
| FF | NOP | ; clear the pipeline |
| 6F | STOP | ; enter STOP Mode |
| | or | |
| FF | NOP | ; clear the pipeline |
| 7F | HALT | ; enter HALT Mode |

STOP. This instruction turns off the internal clock and external crystal oscillation and reduces the standby current to 10 microamperes or less. STOP Mode is terminated by one of the following resets: either by WDT time-out, POR, a Stop-Mode Recovery Source, which is defined by the SMR register or external reset. This causes the processor to restart the application program at address 000CH.

Port Configuration Register (PCON). The PCON register configures the ports individually; comparator output on Port 3, open-drain on Port 0 and Port 1, low EMI on Ports 0, 1, 2 and 3, and low EMI oscillator. The PCON register is located in the expanded register file at Bank F, location 00 (Figure 30).



**Figure 30. Port Configuration Register (PCON)
(Write Only)**

Comparator Output Port 3 (D0). Bit 0 controls the comparator output in Port 3. A “1” in this location brings the comparator outputs to P34 and P37, and a “0” releases the Port to its standard I/O configuration. The default value is 0.

Port 1 Open-Drain (D1). Port 1 can be configured as an open-drain by resetting this bit (D1=0) or configured as push-pull active by setting this bit (D1=1). The default value is 1.

Port 0 Open-Drain (D2). Port 0 can be configured as an open-drain by resetting this bit (D2=0) or configured as push-pull active by setting this bit (D2=1). The default value is 1.

Low EMI Port 0 (D3). Port 0 can be configured as a Low EMI Port by resetting this bit (D3=0) or configured as a Standard Port by setting this bit (D3=1). The default value is 1.

Low EMI Port 1 (D4). Port 1 can be configured as a Low EMI Port by resetting this bit (D4=0) or configured as a Standard Port by setting this bit (D4=1). The default value is 1. **Note:** The emulator does not support Port 1 low EMI mode and must be set D4 = 1.

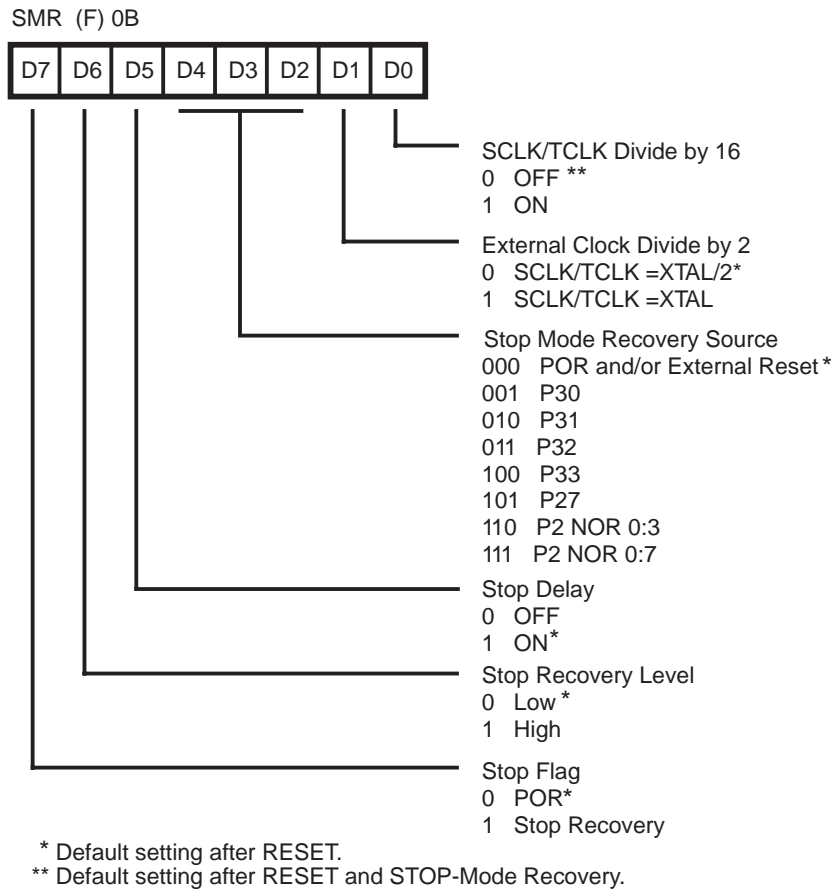
Low EMI Port 2 (D5). Port 2 can be configured as a Low EMI Port by resetting this bit (D5=0) or configured as a Standard Port by setting this bit (D5=1). The default value is 1.

Low EMI Port 3 (D6). Port 3 can be configured as a Low EMI Port by resetting this bit (D6=0) or configured as a Standard Port by setting this bit (D6=1). The default value is 1.

Low EMI OSC (D7). This bit of the PCON Register controls the low EMI noise oscillator. A “1” in this location configures the oscillator with standard drive. While a “0” configures the oscillator with low noise drive, however, it does not affect the relationship of SCLK and XTAL. The low EMI mode will reduce the drive of the oscillator (OSC). The default value is 1. **Note:** 4 MHz is the maximum external clock frequency when running in the low EMI oscillator mode.

Stop-Mode Recovery Register (SMR). This register selects the clock divide value and determines the mode of Stop-Mode Recovery (Figure 31). All bits are Write Only except bit 7 which is a Read Only. Bit 7 is a flag bit that is hardware set on the condition of STOP Recovery and reset by a power-on cycle. Bit 6 controls whether a low or high level is required from the recovery source. Bit 5 controls the reset delay after recovery. Bits 2, 3, and 4 of the SMR register specify the Stop-Mode Recovery Source. The SMR is located in Bank F of the Expanded Register Group at address 0BH.

FUNCTIONAL DESCRIPTION (Continued)



**Figure 31. STOP-Mode Recovery Register
(Write-Only Except Bit D7, Which is Read-Only)**

SCLK/TCLK Divide-by-16 Select (D0). This bit of the SMR controls a divide-by-16 prescaler of SCLK/TCLK. The purpose of this control is to selectively reduce device power consumption during normal processor execution (SCLK control) and/or HALT mode (where TCLK sources counter/timers and interrupt logic).

External Clock Divide-by-Two (D1). This bit can eliminate the oscillator divide-by-two circuitry. When this bit is 0, the System Clock (SCLK) and Timer Clock (TCLK) are equal to the external clock frequency divided by two. The SCLK/TCLK is equal to the external clock frequency when this bit is set (D1=1). Using this bit together with D7 of

PCON further helps lower EMI (i.e., D7 (PCON) = 0, D1 (SMR) = 1). The default setting is zero.

STOP-Mode Recovery Source (D2, D3, and D4). These three bits of the SMR register specify the wake up source of the STOP-Mode Recovery (Figure 32). Table 12 shows the SMR source selected with the setting of D2 to D4. P33–P31 cannot be used to wake up from STOP mode when programmed as analog inputs. When the STOP-Mode Recovery sources are selected in this register then SMR2 register bits D0, D1 must be set to zero.

Note: If the Port2 pin is configured as an output, this output level will be read by the SMR circuitry.



Figure 32. Stop-Mode Recovery Source

FUNCTIONAL DESCRIPTION (Continued)

Table 12. Stop-Mode Recovery Source

| D4 | D3 | D2 | SMR Source selection |
|----|----|----|-------------------------------------|
| 0 | 0 | 0 | POR recovery only |
| 0 | 0 | 1 | P30 transition |
| 0 | 1 | 0 | P31 transition (Not in analog mode) |
| 0 | 1 | 1 | P32 transition (Not in analog mode) |
| 1 | 0 | 0 | P33 transition (Not in analog mode) |
| 1 | 0 | 1 | P27 transition |
| 1 | 1 | 0 | Logical NOR of Port 2 bits 0–3 |
| 1 | 1 | 1 | Logical NOR of Port 2 bits 0–7 |

Stop-Mode Recovery Delay Select (D5). The 5 ms RESET delay after Stop-Mode Recovery is disabled by programming this bit to a zero. A “1” in this bit will cause a 5 ms RESET delay after Stop-Mode Recovery. The default condition of this bit is 1. If the fast wake up mode is selected, the Stop-Mode Recovery source needs to be kept active for at least 5T_{PC}.

Stop-Mode Recovery Level Select (D6). A “1” in this bit defines that a high level on any one of the recovery sources wakes the MCU from STOP Mode. A 0 defines low level recovery. The default value is 0.

Cold or Warm Start (D7). This bit is set by the device upon entering STOP Mode. A “0” in this bit indicates that the device has been reset by POR (cold). A “1” in this bit indicates the device was awakened by a SMR source (warm).

Stop-Mode Recovery Register 2 (SMR2). This register contains additional Stop-Mode Recovery sources. When the Stop-Mode Recovery sources are selected in this register then SMR Register. Bits D2, D3, and D4 must be 0.

| SMR:10 | | Operation |
|--------|----|------------------------------------|
| D1 | D0 | Description of Action |
| 0 | 0 | POR and/or external reset recovery |
| 0 | 1 | Logical AND of P20 through P23 |
| 1 | 0 | Logical AND of P20 through P27 |

Watch-Dog Timer Mode Register (WDTMR). The WDT is a retriggerable one-shot timer that resets the Z8 if it reaches its terminal count. The WDT is disabled after Power-On Reset and initially enabled by executing the WDT instruction and refreshed on subsequent executions of the WDT instruction. The WDT is driven either by an on-board RC oscillator or an external oscillator from XTAL1 pin. The

POR clock source is selected with bit 4 of the WDT register.

Note: Execution of the WDT instruction affects the Z (Zero), S (Sign), and V (Overflow) flags.

WDT Time-Out Period (D0 and D1). Bits 0 and 1 control a tap circuit that determines the time-out periods that can be obtained (Table 13). The default value of D0 and D1 are 1 and 0, respectively.

Table 13. Time-out Period of WDT

| D1 | D0 | Time-out of the Internal RC OSC | Time-out of the System Clock |
|----|----|---------------------------------|------------------------------|
| 0 | 0 | 5 ms | 128 SCLK |
| 0 | 1 | 10 ms* | 256 SCLK* |
| 1 | 0 | 20 ms | 512 SCLK |
| 1 | 1 | 80 ms | 2048 SCLK |

Notes:

*The default setting is 10 ms.

WDT During HALT Mode (D2). This bit determines whether or not the WDT is active during HALT Mode. A “1” indicates that the WDT is active during HALT. A “0” disables the WDT in HALT Mode. The default value is “1”.

WDT During STOP Mode (D3). This bit determines whether or not the WDT is active during STOP mode. A “1” indicates active during STOP. A “0” disables the WDT during STOP Mode. This is applicable only when the WDT clock source is the internal RC oscillator.

Clock Source For WDT (D4). This bit determines which oscillator source is used to clock the internal POR and WDT counter chain. If the bit is a 1, the internal RC oscillator is bypassed and the POR and WDT clock source is driven from the external pin, XTAL1, and the WDT is stopped in STOP Mode. The default configuration of this bit is 0, which selects the RC oscillator.

Permanent WDT. When this feature is enabled, the WDT is enabled after reset and will operate in Run and Halt Mode. The control bits in the WDTMR do not affect the WDT operation. If the clock source of the WDT is the internal RC oscillator, then the WDT will run in STOP mode. If the clock source of the WDT is the XTAL1 pin, then the WDT will not run in STOP mode.

Note: WDT time-out in STOP Mode will not reset SMR, SMR2, PCON, WDTMR, P2M, P3M, Ports 2 & 3 Data Registers.

WDTMR Register Accessibility. The WDTMR register is accessible only during the **first 60** internal system clock

cycles from the execution of the first instruction after Power-On Reset, Watch-Dog reset or a STOP-Mode Recovery (Figures 33 and 34). After this point, the register cannot be modified by any means, intentional or

otherwise. The WDTMR cannot be read and is located in Bank F of the Expanded Register Group at address location 0FH.



* Default setting after RESET

**Figure 33. Watch-Dog Timer Mode Register
Write Only**

FUNCTIONAL DESCRIPTION (Continued)



Figure 34. Resets and WDT

Auto Reset Voltage. An on-board Voltage Comparator checks that V_{CC} is at the required level to ensure correct operation of the device. Reset is globally driven if V_{CC} is below V_{LV} (Figure 35).

Note: V_{CC} must be in the allowed operating range prior to the minimum Power-On Reset time-out (T_{POR}).

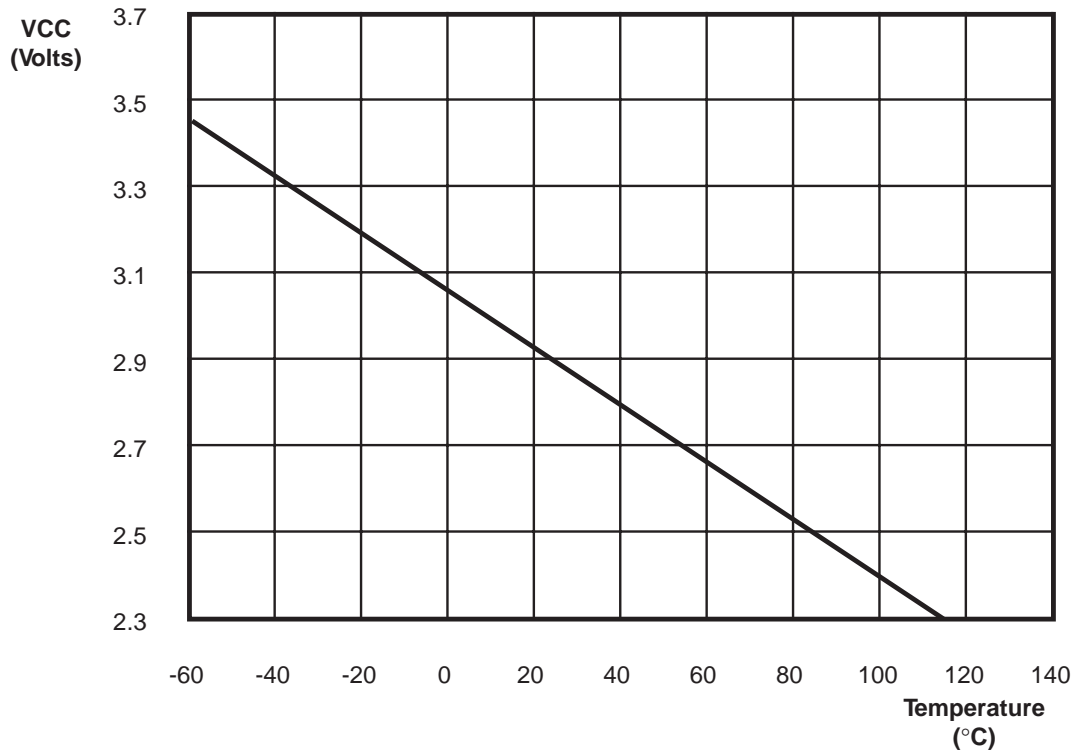


Figure 35. Typical Z86E40 V_{LV} Voltage vs. Temperature

FUNCTIONAL DESCRIPTION (Continued)

EPROM MODE

Table 14 shows the programming voltages of each programming mode. Table 15, and figures that follow show the programming timing of each programming mode. Figure 38 shows the circuit diagram of a Z86E40 programming adapter, which adapts from 2764A to Z86E40 and Figure 39 shows the Z86E30/E31 Programming Adapter Circuitry. Figure 40 shows the flowchart of an Intelligent Programming Algorithm, which is compatible with 2764A EPROM (Z86E40 is 4K EPROM, 2764A is 8K EPROM). Since the EPROM size of Z86E30/E31/E40 differs from 2764A, the programming address range has to be set from 0000H to 0FFFH for the Z86E30/E40 and 0000H to 07FFH for Z86E31. Otherwise, the upper portion of EPROM data will overwrite the lower portion of EPROM data. Figure 39 shows the adaptation from the 2764A to Z86E30/E31.

Note: EPROM Protect feature allows the LDC, LDCI, LDE, and LDEI instructions from internal program memory. A ROM lookup table can be used with this feature.

During programming, the V_{PP} input pin supplies the programming voltage and current to the EPROM. This pin is also used to latch which EPROM mode is to be used (R/W EPROM or R/W Option bits). The mode is set by placing the correct mode number on the least significant bits of the address and raising the EPM pin above V . After a setup time, the V_{PP} pin can then be raised or lowered. The latched EPROM mode will remain until the EPM pin is reduced below V_H .

| Mode Name | Mode # | LSB Addr |
|----------------|--------|----------|
| EPROM R/W | 0 | 0000 |
| Option Bit R/W | 3 | 0011 |

EPROM R/W mode allows the programming of the user mode program ROM.

Option Bit R/W allows the programming of the Z8 option bits. When the device is latched into Option Bit R/W mode, the address must then be changed to 63 decimals (000000111111 Binary). The Options are mapped into this address as follows:

| Bit | Option |
|-----|----------------------|
| 7 | Unused |
| 6 | Unused |
| 5 | 32 KHz XTAL Option |
| 4 | Permanent WDT |
| 3 | Auto Latch Disable |
| 2 | RC Oscillator Option |
| 1 | RAM Protect |
| 0 | ROM Protect |

Table 14 gives the proper conditions for EPROM R/W operations, once the mode is latched.

Table 14. EPROM Programming Table

| Programming Modes | V _{PP} | EPM | \overline{CE} | \overline{OE} | \overline{PGM} | ADDR | DATA | V _{CC} * |
|-------------------|-----------------|----------------|-----------------|-----------------|------------------|------|------|-------------------|
| EPROM READ1 | X | V _H | V _{IL} | V _{IL} | V _{IH} | ADDR | Out | 4.5V† |
| EPROM READ2 | X | V _H | V _{IL} | V _{IL} | V _{IH} | ADDR | Out | 5.5V† |
| PROGRAM | V _H | V _H | V _{IL} | V _{IH} | V _{IL} | ADDR | In | 6.4V |
| PROGRAM VERIFY | V _H | V _H | V _{IL} | V _{IL} | V _{IH} | ADDR | Out | 6.0V |
| OPTION BIT PGM | V _H | V _H | V _{IL} | V _{IH} | V _{IL} | 63 | IN | 6.4V |
| OPTION BIT READ | X | V _H | V _{IL} | V _{IL} | V _{IH} | 63 | OUT | 6.0V |

Notes:V_H = 13.0 V ± 0.1 VV_{IH} = As per specific Z8 DC specificationV_{IL} = As per specific Z8 DC specificationX=Not used, but must be set to V_H, V_{IH}, or V_{IL} level.NU = Not used, but must be set to either V_{IH} or V_{IL} level.I_{PP} during programming = 40 mA maximum.I_{CC} during programming, verify, or read = 40 mA maximum.*V_{CC} has a tolerance of ±0.25V.

† Zilog recommends an EPROM read at V_{CC} = 4.5 V and 5.5 V to ensure proper device operations during the V_{CC} after programming, but V_{CC} = 5.0 V is acceptable.

Table 15. EPROM Programming Timing

| Parameters | Name | Min | Max | Units |
|------------|--|------|------|-------|
| 1 | Address Setup Time | 2 | | μs |
| 2 | Data Setup Time | 2 | | μs |
| 3 | V _{PP} Setup | 2 | | μs |
| 4 | V _{CC} Setup Time | 2 | | μs |
| 5 | Chip Enable Setup Time | 2 | | μs |
| 6 | Program Pulse Width | 0.95 | 1.05 | ms |
| 7 | Data Hold Time | 2 | | μs |
| 8 | \overline{OE} Setup Time | 2 | | μs |
| 9 | Data Access Time | 200 | | ns |
| 10 | Data Output Float Time | | 100 | ns |
| 11 | Overprogram Pulse Width/Option Program Pulse Width | 2.85 | | ms |
| 12 | EPM Setup Time | 2 | | μs |
| 13 | \overline{PGM} Setup Time | 2 | | μs |
| 14 | Address to \overline{OE} Setup Time | 2 | | μs |
| 15 | \overline{OE} Width | 250 | | ns |
| 16 | Address to \overline{OE} Low | 125 | | ns |

FUNCTIONAL DESCRIPTION (Continued)



Figure 36. EPROM Read Mode Timing Diagram

Z86E40 TIMING DIAGRAMS

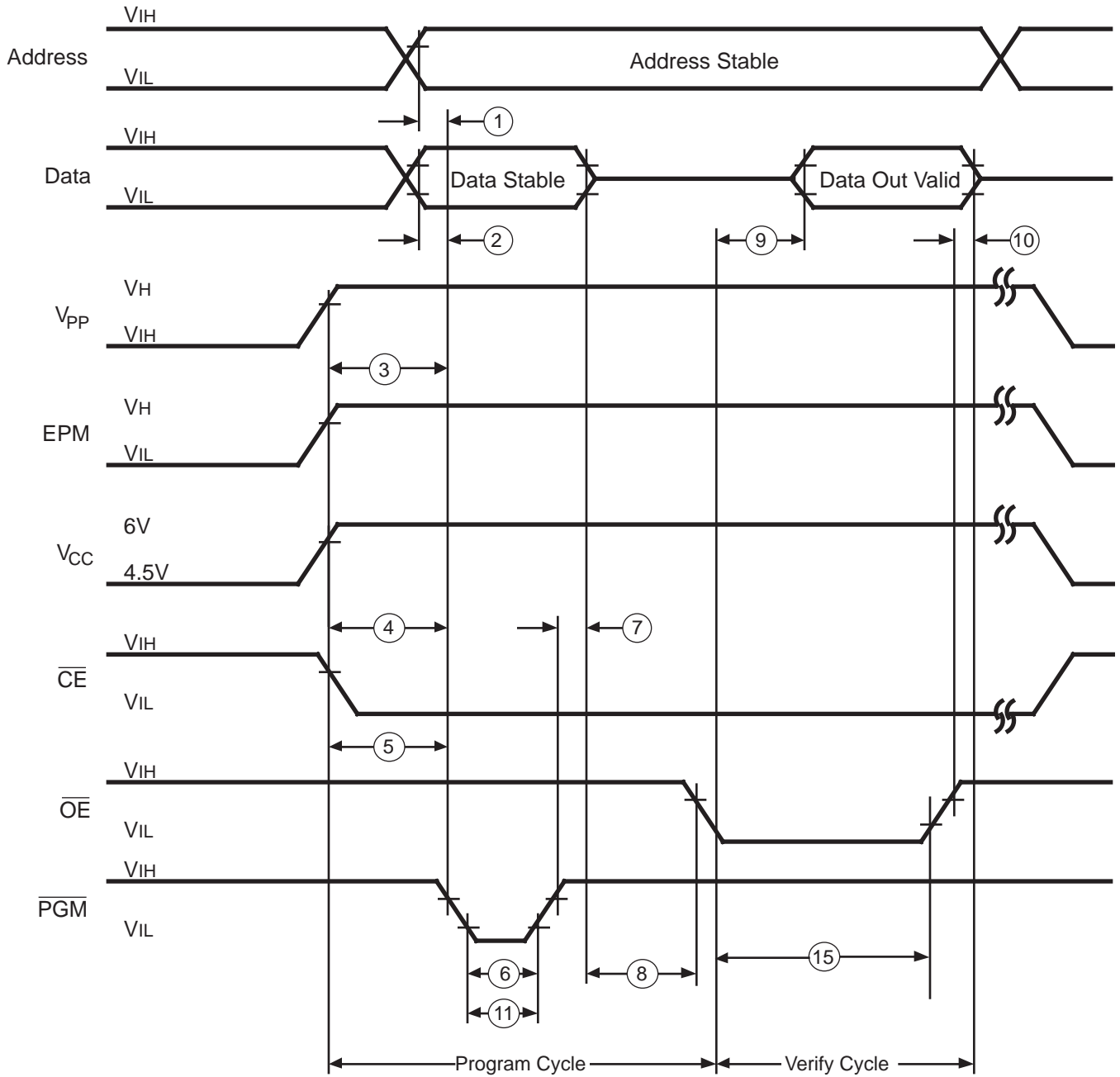


Figure 37. Timing Diagram of EPROM Program and Verify Modes

Z86E40 TIMING DIAGRAMS (Continued)



Z86E40
40-Pin DIP
Socket

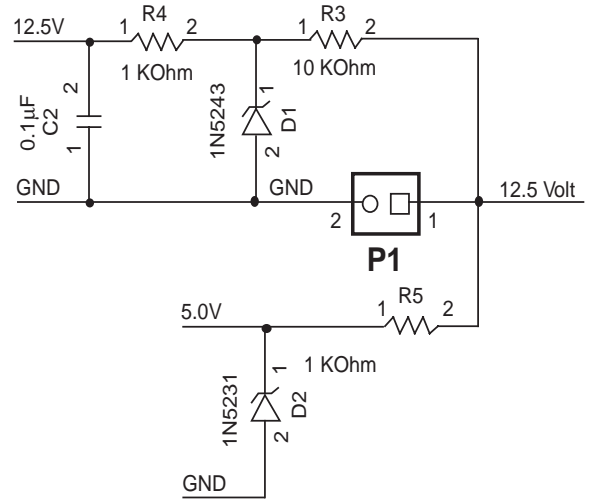


Figure 38. Z86E40 Z8 OTP Programming Adapter
For use with Standard EPROM Programmers



Figure 39. Z86E30/E31 Programming Adapter Circuitry



Figure 40. Z86E40 Programming Algorithm

EXPANDED REGISTER FILE CONTROL REGISTERS

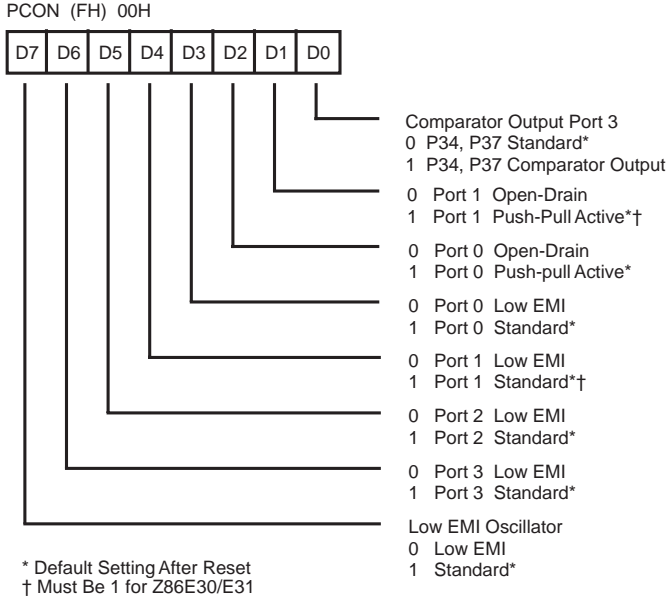


Figure 41. Port Configuration Register
Write Only

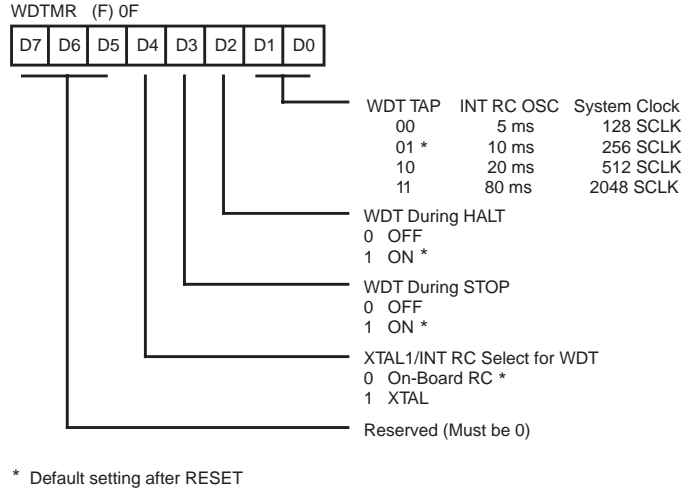


Figure 43. Watch-Dog Timer Mode Register
Write Only



Figure 42. STOP-Mode Recovery Register
Write Only Except Bit D7, Which is Read Only



Figure 44. STOP-Mode Recovery Register 2
Write Only

Z8 CONTROL REGISTER DIAGRAMS



Figure 45. Reserved



Default After Reset = 00H

Figure 46. Timer Mode Register
F1H: Read/Write



Figure 47. Counter/Timer 1 Register
F2H: Read/Write



*Default After Reset

Figure 48. Prescaler 1 Register
F3H: Write Only

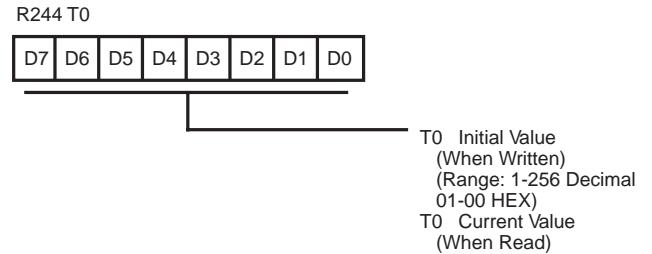
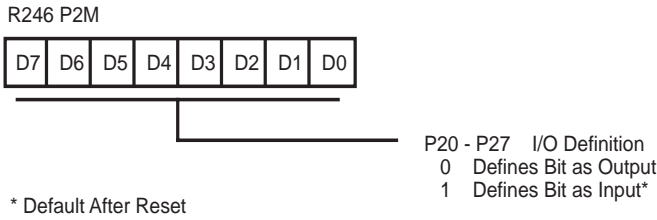


Figure 49. Counter/Timer 0 Register
F4H; Read/Write

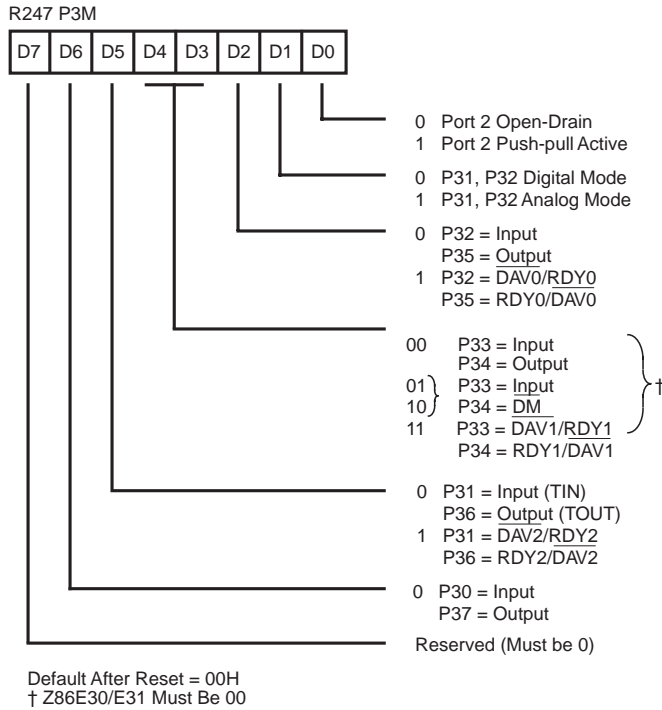


Figure 50. Prescaler 0 Register
F5H: Write Only

Z8 CONTROL REGISTER DIAGRAMS (Continued)



**Figure 51. Port 2 Mode Register
F6H: Write Only**



**Figure 52. Port 3 Mode Register
F7H: Write Only**



**Figure 53. Port 0 and 1 Mode Register
F8H: Write Only
Z86E30/E31 Only**



**Figure 54. Interrupt Priority Register
F9H: Write Only**

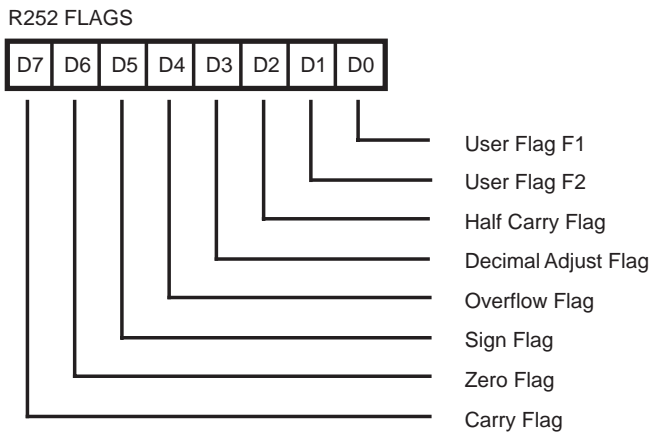


**Figure 55. Interrupt Request Register
FAH: Read/Write**



† This option must be selected when ROM code is submitted for ROM Masking, otherwise this control bit is disabled permanently.

**Figure 56. Interrupt Mask Register
FBH: Read/Write**



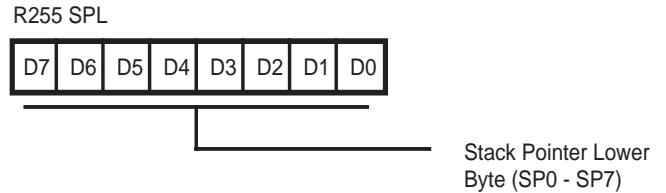
**Figure 57. Flag Register
FCH: Read/Write**



**Figure 58. Register Pointer
FDH: Read/Write**



**Figure 59. Stack Pointer High
FEH: Read/Write**



**Figure 60. Stack Pointer Low
FFH: Read/Write**

PACKAGE INFORMATION (Continued)

PACKAGE INFORMATION

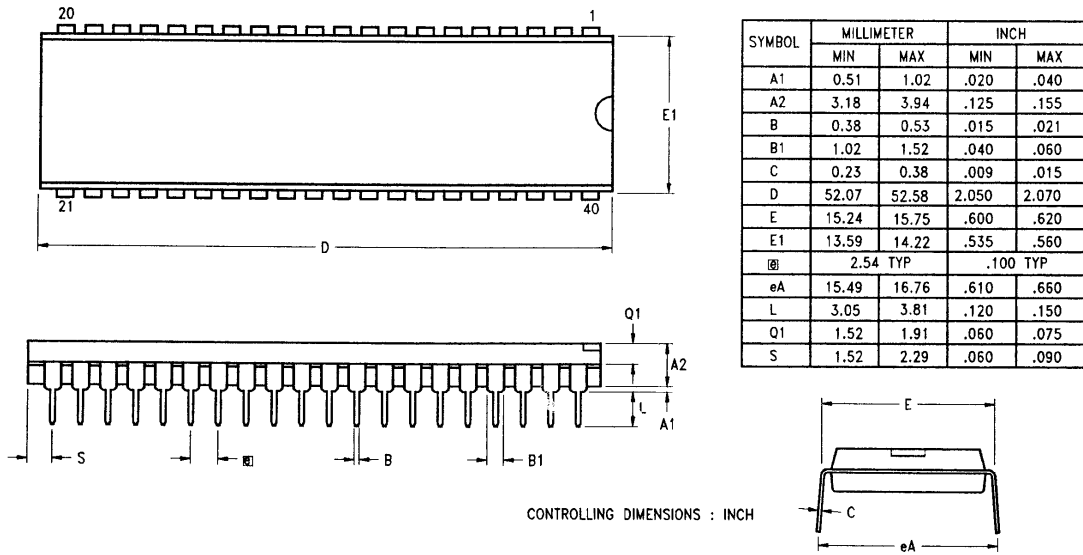


Figure 61. 40-Pin DIP Package Diagram



NOTES:

1. CONTROLLING DIMENSIONS : INCH
2. LEADS ARE COPLANAR WITHIN .004 IN.
3. DIMENSION : $\frac{\text{MM}}{\text{INCH}}$

| SYMBOL | MILLIMETER | | INCH | |
|--------|------------|-------|----------|------|
| | MIN | MAX | MIN | MAX |
| A | 4.27 | 4.57 | .168 | .180 |
| A1 | 2.41 | 2.92 | .095 | .115 |
| D/E | 17.40 | 17.65 | .685 | .695 |
| D1/E1 | 16.51 | 16.66 | .650 | .656 |
| D2 | 15.24 | 16.00 | .600 | .630 |
| Ⓜ | 1.27 TYP | | .050 TYP | |

Figure 62. 44-Pin PLCC Package Diagram



- NOTES:
1. CONTROLLING DIMENSIONS : MILLIMETER
 2. LEAD COPLANARITY : MAX .10
.004"

Figure 63. 44-Pin LQFP Package Diagram



Figure 64. 28-Pin DIP Package Diagram



Figure 65. 28-Pin SOIC Package Diagram



Figure 66. 28-Pin PLCC Package Diagram

ORDERING INFORMATION

Z86E40 (16 MHz)

| 40-Pin DIP | 44-Pin PLCC | 44-Pin LQFP |
|-------------|-------------|-------------|
| Z86E4016PSC | Z86E4016VSC | Z86E4016FSC |
| Z86E4016PEC | Z86E4016VEC | Z86E4016FEC |

Z86E30 (16 MHz)

| 28-Pin DIP | 28-Pin SOIC | 28-Pin PLCC |
|-------------|-------------|-------------|
| Z86E3016PSC | Z86E3016SSC | Z86E3016VSC |
| Z96E3016PEC | Z86E3016SEC | Z86E3016VEC |

Z86E31 (16 MHz)

| 28-Pin DIP | 28-Pin SOIC | 28-Pin PLCC |
|-------------|-------------|-------------|
| Z86E3116PSC | Z86E3116SSC | Z86E3116VSC |
| Z86E3116PEC | Z86E3116SEC | Z86E3116VEC |

For fast results, contact your local Zilog sales office for assistance in ordering the part desired.

Package

P = Plastic DIP

V = Plastic Leaded Chip Carrier

F = Plastic Quad Flat Pack

S = SOIC (Small Outline Integrated Circuit)

Temperature

S = 0 °C to +70 °C

E = -40 °C to +105 °C

Speed

16 = 16 MHz

Environmental

C = Plastic Standard

E = Hermetic Standard

Example:

Z 86E40 16 P S C is a Z86E40, 16 MHz, DIP, 0°C to +70°C, Plastic Standard Flow



Customer Support

For answers to technical questions about the product, documentation, or any other issues with Zilog's offerings, please visit Zilog's Knowledge Base at <http://www.zilog.com/kb>.

For any comments, detail technical questions, or reporting problems, please visit Zilog's Technical Support at <http://support.zilog.com>.

Компания «Океан Электроники» предлагает заключение долгосрочных отношений при поставках импортных электронных компонентов на взаимовыгодных условиях!

Наши преимущества:

- Поставка оригинальных импортных электронных компонентов напрямую с производств Америки, Европы и Азии, а так же с крупнейших складов мира;
- Широкая линейка поставок активных и пассивных импортных электронных компонентов (более 30 млн. наименований);
- Поставка сложных, дефицитных, либо снятых с производства позиций;
- Оперативные сроки поставки под заказ (от 5 рабочих дней);
- Экспресс доставка в любую точку России;
- Помощь Конструкторского Отдела и консультации квалифицированных инженеров;
- Техническая поддержка проекта, помощь в подборе аналогов, поставка прототипов;
- Поставка электронных компонентов под контролем ВП;
- Система менеджмента качества сертифицирована по Международному стандарту ISO 9001;
- При необходимости вся продукция военного и аэрокосмического назначения проходит испытания и сертификацию в лаборатории (по согласованию с заказчиком);
- Поставка специализированных компонентов военного и аэрокосмического уровня качества (Xilinx, Altera, Analog Devices, Intersil, Interpoint, Microsemi, Actel, Aeroflex, Peregrine, VPT, Syfer, Eurofarad, Texas Instruments, MS Kennedy, Miteq, Cobham, E2V, MA-COM, Hittite, Mini-Circuits, General Dynamics и др.);

Компания «Океан Электроники» является официальным дистрибьютором и эксклюзивным представителем в России одного из крупнейших производителей разъемов военного и аэрокосмического назначения «JONHON», а так же официальным дистрибьютором и эксклюзивным представителем в России производителя высокотехнологичных и надежных решений для передачи СВЧ сигналов «FORSTAR».



JONHON

«JONHON» (основан в 1970 г.)

Разъемы специального, военного и аэрокосмического назначения:

(Применяются в военной, авиационной, аэрокосмической, морской, железнодорожной, горно- и нефтедобывающей отраслях промышленности)

«FORSTAR» (основан в 1998 г.)

ВЧ соединители, коаксиальные кабели, кабельные сборки и микроволновые компоненты:

(Применяются в телекоммуникациях гражданского и специального назначения, в средствах связи, РЛС, а так же военной, авиационной и аэрокосмической отраслях промышленности).



Телефон: 8 (812) 309-75-97 (многоканальный)

Факс: 8 (812) 320-03-32

Электронная почта: ocean@oceanchips.ru

Web: <http://oceanchips.ru/>

Адрес: 198099, г. Санкт-Петербург, ул. Калинина, д. 2, корп. 4, лит. А