MP4575

5A, 4.5V - 55V Input, Frequency-Programmable, Fully Integrated, Synchronous, Step-Down Converter

The Future of Analog IC Technology

DESCRIPTION

The MP4575 is a frequency-programmable, step-down, switching converter with integrated, internal, high-side and low-side power MOSFETs. The MP4575 can provide 5A of continuous output current with peak current control for excellent transient response and efficiency performance.

The wide 4.5V to 55V input voltage range accommodates a variety of step-down applications, including industrial, PoE, automotive, and printers with a DC high-voltage bus.

The MP4575 uses peak-current-mode control to regulate the output voltage. The MP4575 provides over-current protection (OCP) with valley current detection, which is used to prevent the current from running away. The MP4575 also has accurate and reliable over-voltage protection (OVP) and auto-recovery thermal protection.

An optional external soft start is available. Enable and power good indication functions can be used to track the power easily. To increase efficiency, the MP4575 scales down the switching frequency automatically when the load is light. Meanwhile, the low-side MOSFET is turned off to reduce driver loss when zero inductor current is detected.

Synchronous operation mode with the integrated low-side MOSFET is useful for reducing conduction loss and reducing external components space to save cost.

The MP4575 is available in a TSSOP-20 EP package with an exposed pad.

FEATURES

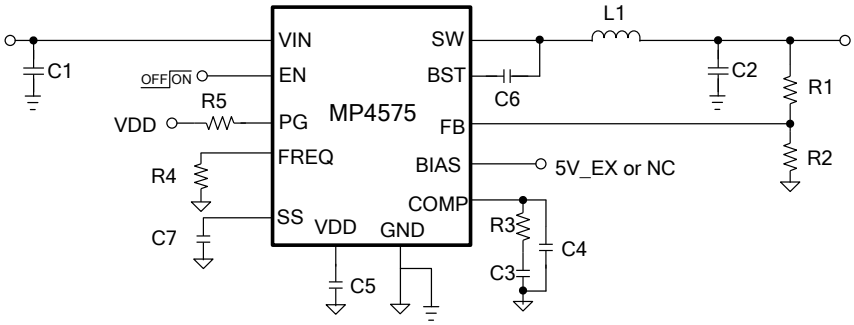
- Wide 4.5V to 55V Input Voltage Range
- 90mΩ and 70mΩ Internal High-Side and Low-Side Power MOSFETs
- Peak-Current-Mode Control
- Programmable Switching Frequency
- Optional External Soft Start
- Over-Current Protection (OCP) with Valley Current Detection
- Supports External Synchronous Clock
- Over-Voltage Protection (OVP)
- Current Limit Decreases during Output Short for Better Thermal Performance
- Power Good Indication
- Thermal Shutdown Protection
- Available in a TSSOP-20 EP Package

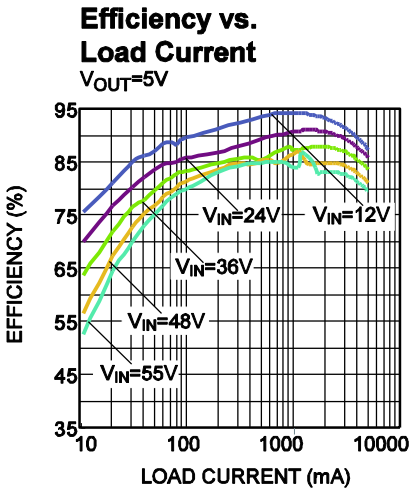
APPLICATIONS

- PoE Input Non-Isolated Buck
- Industrial Power Systems
- Printers and Scanners
- Automotive Power Systems
- Distributed Power Systems

All MPS parts are lead-free, halogen-free, and adhere to the RoHS directive. For MPS green status, please visit the MPS website under Quality Assurance. “MPS” and “The Future of Analog IC Technology” are registered trademarks of Monolithic Power Systems, Inc.

TYPICAL APPLICATION





ORDERING INFORMATION

Part Number*	Package	Top Marking
MP4575GF	TSSOP-20 EP	*See Below*

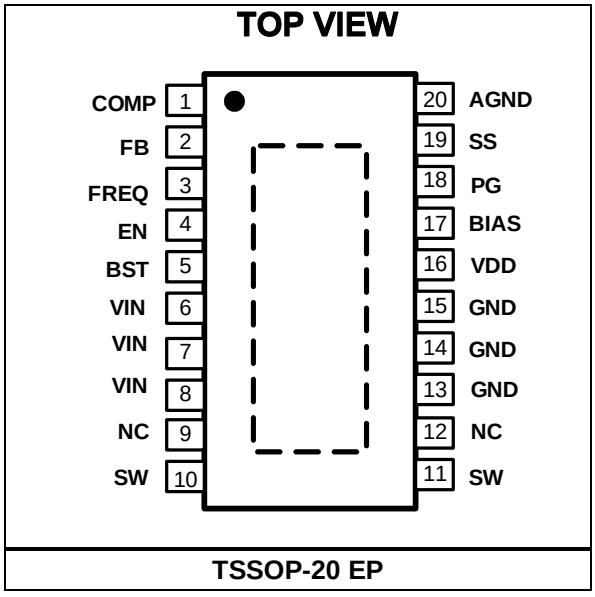
* For Tape & Reel, add suffix –Z (e.g. MP4575GF–Z)

TOP MARKING

MPSYYWW
MP4575
LLLLLLLLL

MPS: MPS prefix
YY: Year code
WW: Week code
MP4575: Product code of MP4575GF
LLLLLLLLL: Lot number

PACKAGE REFERENCE



TSSOP-20 EP

ABSOLUTE MAXIMUM RATINGS (1)

Supply voltage (VIN) 60V
V_{SW} ..... -0.5V to (VIN + 0.5V)
V_{BS} ..... V_{SW} + 6V
All other pins ..... -0.3V to +6V
EN sink current 150µA
Continuous power dissipation (T_A = 25°C) (2)
TSSOP-20 EP 2.78W
Junction temperature ..... 150°C
Lead temperature ..... 260°C
Storage temperature ..... -65°C to +150°C

Recommended Operating Conditions

Supply voltage (VIN) ..... 4.5V to 55V
Output voltage (V_{OUT}) ..... 1V to 0.9xVIN
Operating junction temp. (T_J). .. -40°C to +125°C

Thermal Resistance (3) θ_{JA} θ_{JC}

	θ_{JA}	θ_{JC}	
TSSOP-20 EP	45	10	°C/W

NOTES:

1) Absolute maximum ratings are rated under room temperature unless otherwise noted. Exceeding these ratings may damage the device.
2) The maximum allowable power dissipation is a function of the maximum junction temperature TJ (MAX), the junction-to-ambient thermal resistance θJA, and the ambient temperature TA. The maximum allowable continuous power dissipation at any ambient temperature is calculated by PD (MAX) = (TJ (MAX)-TA)/θJA. Exceeding the maximum allowable power dissipation produces an excessive die temperature, causing the regulator to go into thermal shutdown. Internal thermal shutdown circuitry protects the device from permanent damage.
3) Measured on JESD51-7, 4-layer PCB.

ELECTRICAL CHARACTERISTICS

V_{IN} = 48V, V_{EN} = 3.3V, T_J = 25°C, unless otherwise noted.

Parameter	Symbol	Condition	Min	Typ	Max	Units
Error Amplifier (EA)						
Feedback voltage	V_{FB}	4.5V ≤ VIN ≤ 55V	0.98	1	1.02	V
FB current	I_{FB}	V_{FB} = 1.07V		10	50	nA
Error amp transconductance			380	540	720	μA/V
COMP sink/source current	I_{COMP}		10	20	30	μA
Switch Characteristic						
Upper switch on resistance	R_{ON_HS}			90	160	mΩ
Lower switch on resistance	R_{ON_LS}			70	120	mΩ
Upper switch leakage	I_{LKG_SW}	V_{EN} = 0V, V_{SW} = 0V		10	300	nA
Current Limit						
Peak current limit	I_{LIMIT}	10% duty cycle	5.5	8.5	11	A
Quiescent Supply						
Quiescent supply current	I_Q	No load, without switching		450	670	μA
Shutdown supply current	I_{SHDN}	V_{EN} = 0V		7	12	μA
VDD Regulator						
VDD regulator output voltage	V_{DD}	BIAS = NC	3.4	3.6	3.8	V
VDD regulator output voltage	V_{DD}	BIAS = external 5V power	4.6	4.8		V
Threshold Voltage						
EN rising threshold	V_{EN_R}		1.4	1.6	1.8	V
EN falling threshold	V_{EN_F}		1.1	1.3	1.5	V
EN threshold hysteresis	V_{EN_HYS}			300		mV
VIN UVLO rising threshold	V_{INUV_R}		3.7	3.9	4.1	V
VIN UVLO falling threshold	V_{INUV_F}		3.3	3.5	3.7	V
VIN UVLO threshold hysteresis	V_{INUV_HYS}			400		mV
Soft Start (SS)						
External soft start capacitor charging current	I_{SS}	V_{SS} = 1V	2.5	4	5.5	μA
PWM Comparator						
Minimum off time (4)	t_{OFF_MIN}			100		ns
Minimum on time (4)	t_{ON_MIN}			90		ns

ELECTRICAL CHARACTERISTICS *(continued)*

V_{IN} = 48V, V_{EN} = 3.3V, T_J = 25°C, unless otherwise noted.

Parameter	Symbol	Condition	Min	Typ	Max	Units
Oscillator Frequency						
Switching frequency	f_{SW}	R_{FREQ} = 100kΩ	400	520	640	kHz
Over-Voltage Protection (OVP)						
Output OVP threshold	V_{OVP}	$V_{FB(OVP)}/V_{FB}$	108	115	122	%
Power Good (PG)						
Power good threshold	V_{PG_TH}	V_{OUT} rising, $V_{FB(PG)}/V_{FB}$	86	90	94	%
		V_{OUT} falling, $V_{FB(PG)}/V_{FB}$	81	85	89	
Power good hysteresis	V_{PG_HYS}	$\Delta V_{FB(PG)}/V_{FB}$		5		%
Power good delay	t_{PG_DL}	V_{OUT} rising	8	22	37	µs
		V_{OUT} falling	8	21	33	µs
Frequency SYNC						
SYNC leakage current	I_{LKG_SYNC}			10	100	nA
SYNC frequency range	f_{SYNC}		100		1000	kHz
Thermal						
Thermal shutdown (4)	T_{SD}		150	170		°C
Thermal shutdown hysteresis (4)	T_{SD_HYS}			10		°C

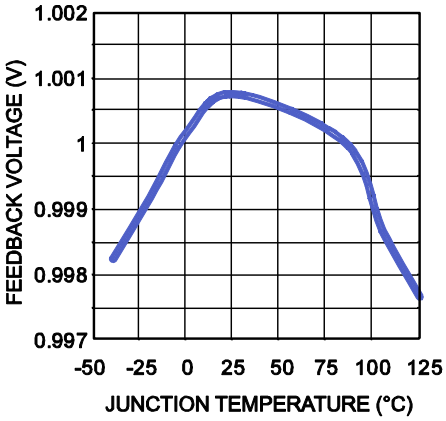
NOTE:

4) Derived from bench characterization. Not tested in production.

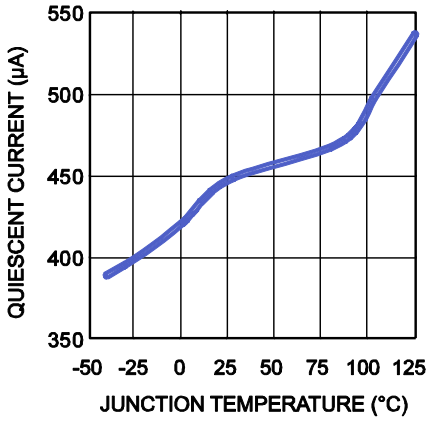
TYPICAL CHARACTERISTICS

V_{IN} = 48V, unless otherwise noted.

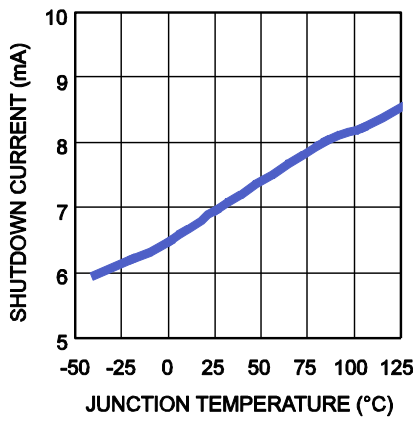
Feedback Voltage vs. Junction Temperature



Quiescent Current vs. Junction Temperature

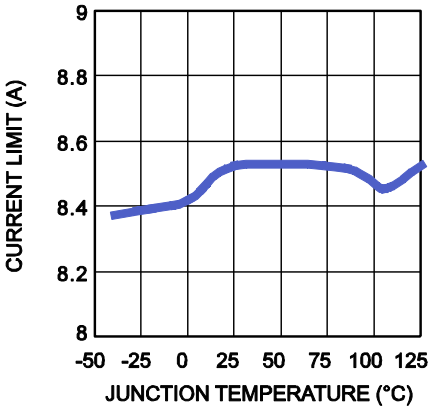


Shutdown Current vs. Junction Temperature

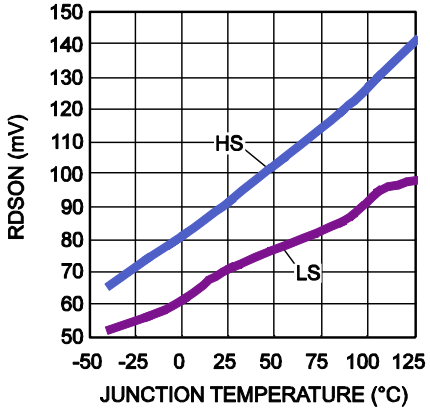


Current Limit vs. Junction Temperature

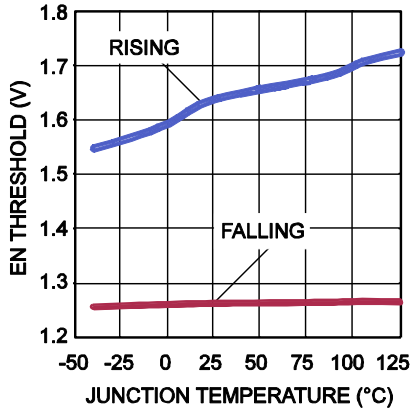
Duty Cycle=10%



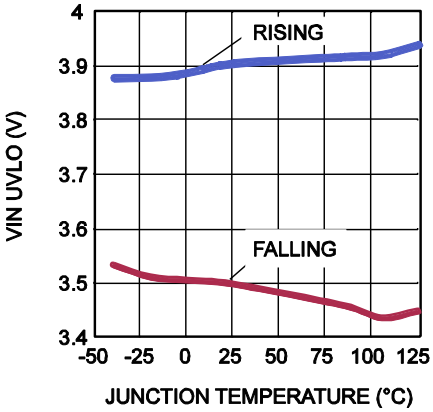
Switch ON Resistance vs. Junction Temperature



EN Threshold vs. Junction Temperature

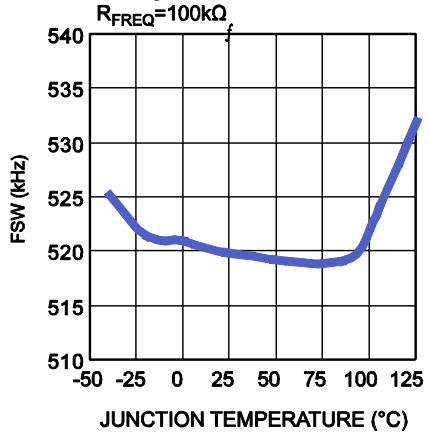


V_{IN} UVLO vs. Junction Temperature



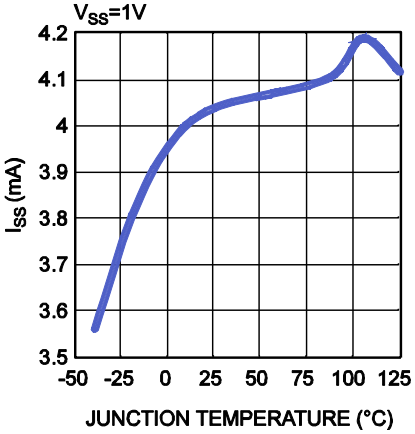
f_{SW} vs. Junction Temperature

R_{FREQ}=100kΩ



I_{SS} vs. Junction Temperature

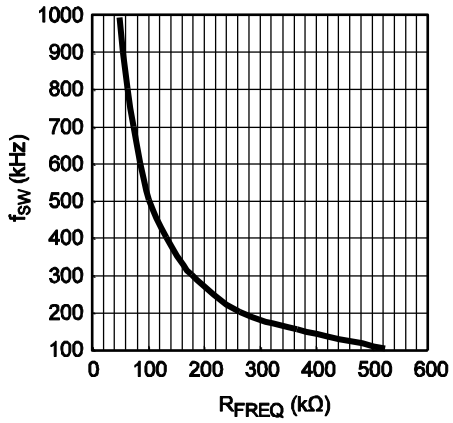
V_{SS}=1V



TYPICAL CHARACTERISTICS *(continued)*

V_{IN} = 48V, unless otherwise noted.

f_{SW} vs. R_{FREQ}

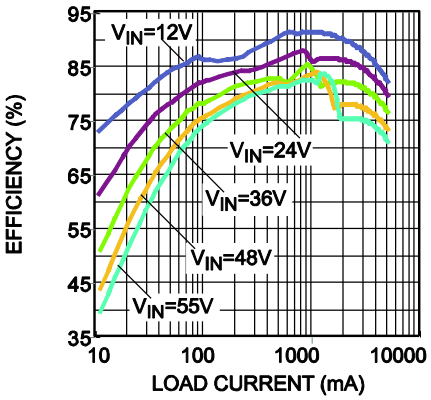


TYPICAL PERFORMANCE CHARACTERISTICS

V_{IN} = 48V, V_{OUT} = 3.3V, C_{OUT} = 2x22µF, L = 10µH, f_{SW} = 500kHz, T_A = +25°C, unless otherwise noted.

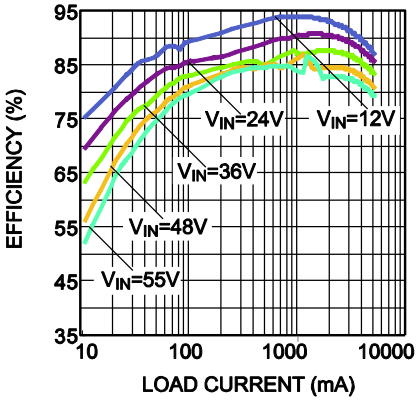
Efficiency vs. Load Current

V_{OUT}=3.3V

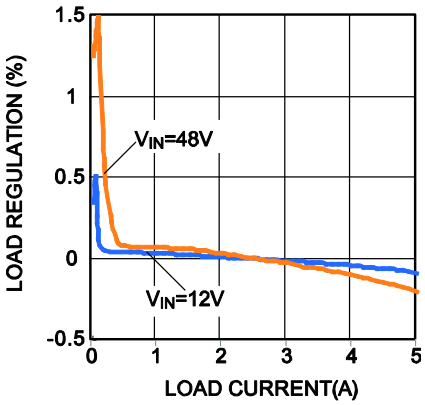


Efficiency vs. Load Current

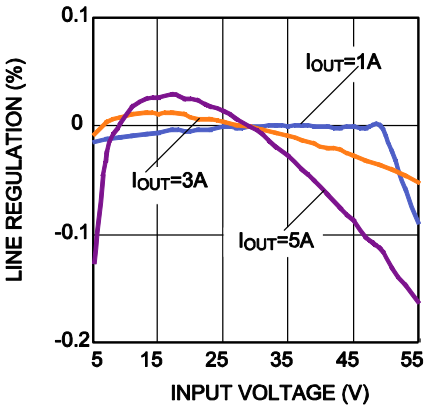
V_{OUT}=5V



Load Regulation



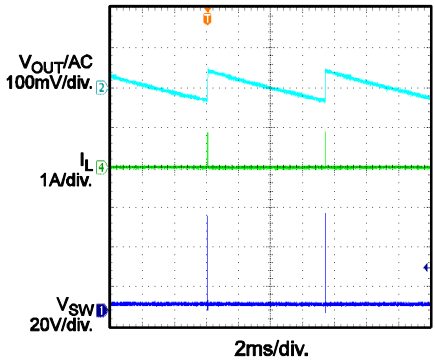
Line Regulation



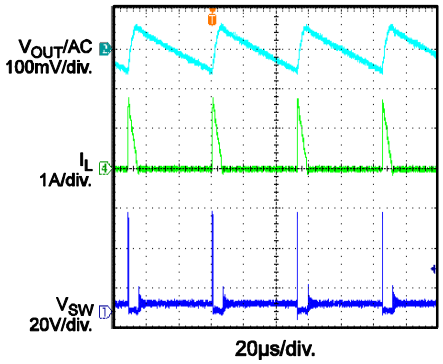
TYPICAL PERFORMANCE CHARACTERISTICS *(continued)*

V_{IN} = 48V, V_{OUT} = 3.3V, C_{OUT} = 2x22µF, L = 10µH, f_{SW} = 500kHz, T_A = +25°C, unless otherwise noted.

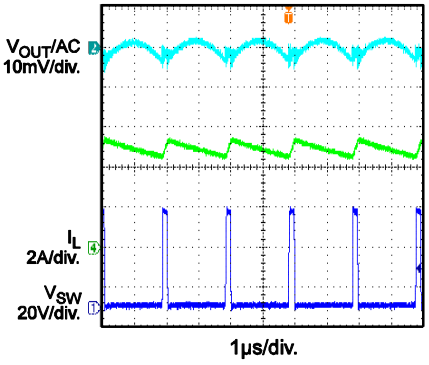
Steady State
I_{OUT}=0A



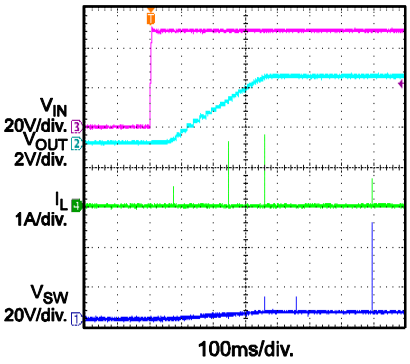
Steady State
I_{OUT}=0.1A



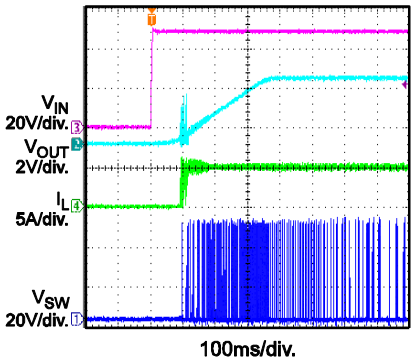
Steady State
I_{OUT}=5A



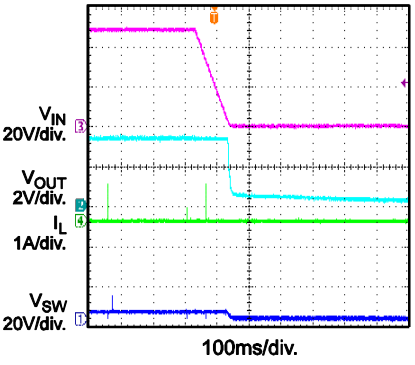
Startup Through V_{IN}
I_{OUT} = 0A



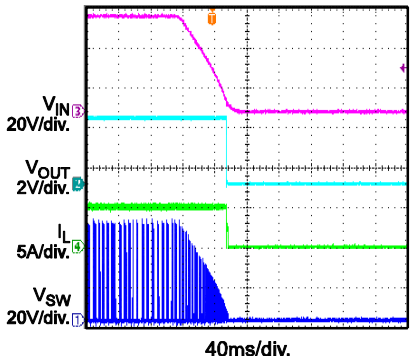
Startup Through V_{IN}
I_{OUT} = 5A



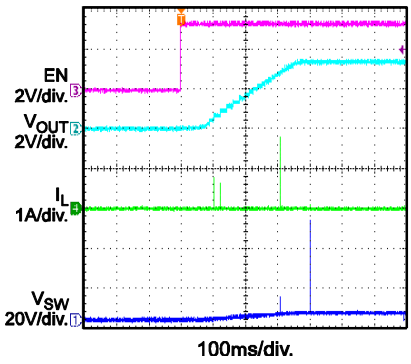
Shutdown Through V_{IN}
I_{OUT} = 0A



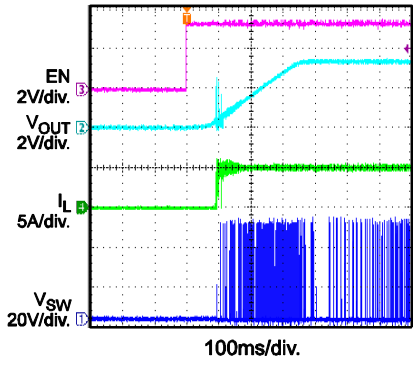
Shutdonw Through V_{IN}
I_{OUT} = 5A



Startup Through EN
I_{OUT} = 0A



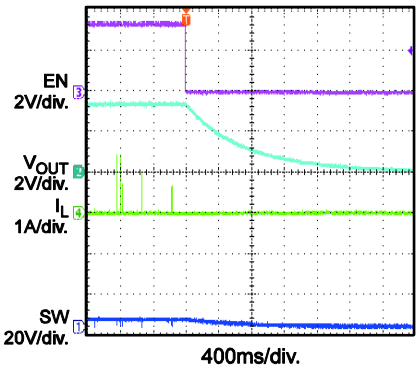
Startup Through EN
I_{OUT} = 5A



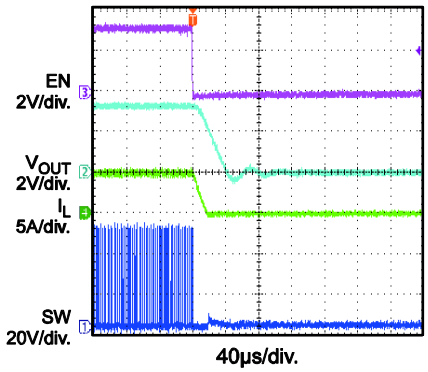
TYPICAL PERFORMANCE CHARACTERISTICS *(continued)*

V_{IN} = 48V, V_{OUT} = 3.3V, C_{OUT} = 2x22µF, L = 10µH, f_{SW} = 500kHz, T_A = +25°C, unless otherwise noted.

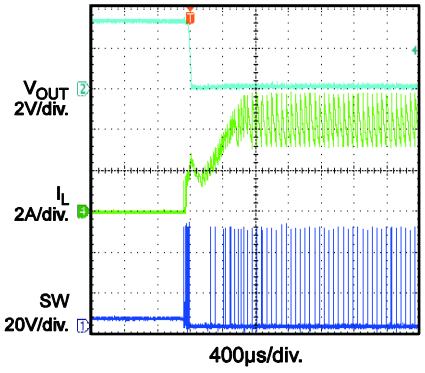
Shutdown Through EN
I_{OUT}=0A



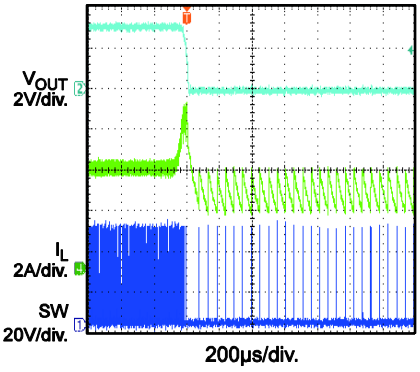
Shutdown Through EN
I_{OUT}=5A



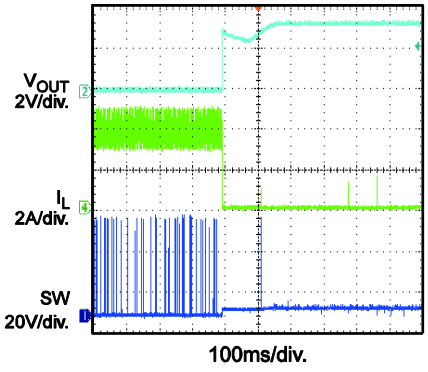
SCP Entry
I_{OUT}=0A to Short Circuit



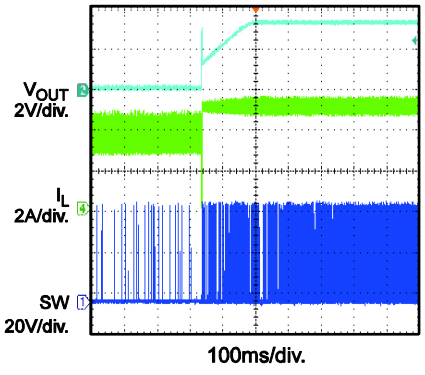
SCP Entry
I_{OUT}=5A to Short Circuit



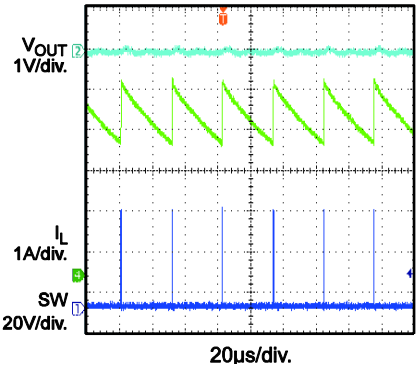
SCP Recovery
I_{OUT}= Short Circuit to 0A



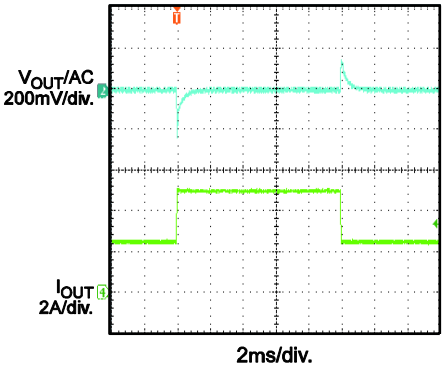
SCP Recovery
I_{OUT}=Short Circuit to 5A



SCP Steady State



Load Transient
I_{OUT} =2.5A <-> 5A, 160mA/µs



PIN FUNCTIONS

Pin #	Name	Description
1	COMP	**Compensation network setting.** Connect an external resistor in series with a capacitor between COMP and GND.
2	FB	**Feedback.** FB is the input to the PWM comparator. Place an external resistor divider between the output and GND.
3	FREQ	**Switching frequency setting.** Connect a resistor from FREQ to GND to set the switching frequency. If an external synchronous clock is applied to FREQ, the converter follows this clock's frequency.
4	EN	**Enable input.** Pull EN below the specified threshold to shut down the MP4575. There is no internal pull-up or pull-down circuit. Do not float EN.
5	BST	**Bootstrap.** BST is the positive power supply for the internal floating high-side MOSFET driver. Connect a capacitor between BST and SW.
6, 7, 8	VIN	**Input supply.** VIN supplies power to all of the internal control circuitries and VDD regulator. A decoupling capacitor to ground must be placed close to VIN to minimize switching spikes.
9, 12	NC	**No connection.** Leave NC floating.
10, 11	SW	**Switch node.** SW is the output node from the internal high-side MOSFET source.
13, 14, 15, Exposed Pad	GND	**Power ground for the internal power MOSFETs.**
16	VDD	**Power for the internal MOSFET driver and BST charging circuit.**
17	BIAS	**Optional supply for the internal circuit.** For better thermal performance, connect BIAS to an external 5V source. VDD and the internal circuit are powered by BIAS. Since there is a diode between BIAS and the internal circuit, leave BIAS floating or connect it to GND if BIAS is not used.
18	PG	**Power good indicator.** Connect a resistor to a pull-up power source if used.
19	SS	**Optional external soft-start time setting.** Connect an external capacitor between SS and GND to set the soft-start time externally. Float SS to activate the internal 0.5ms soft-start setting.
20	AGND	**Ground for internal logic and signal circuit.**

BLOCK DIAGRAM

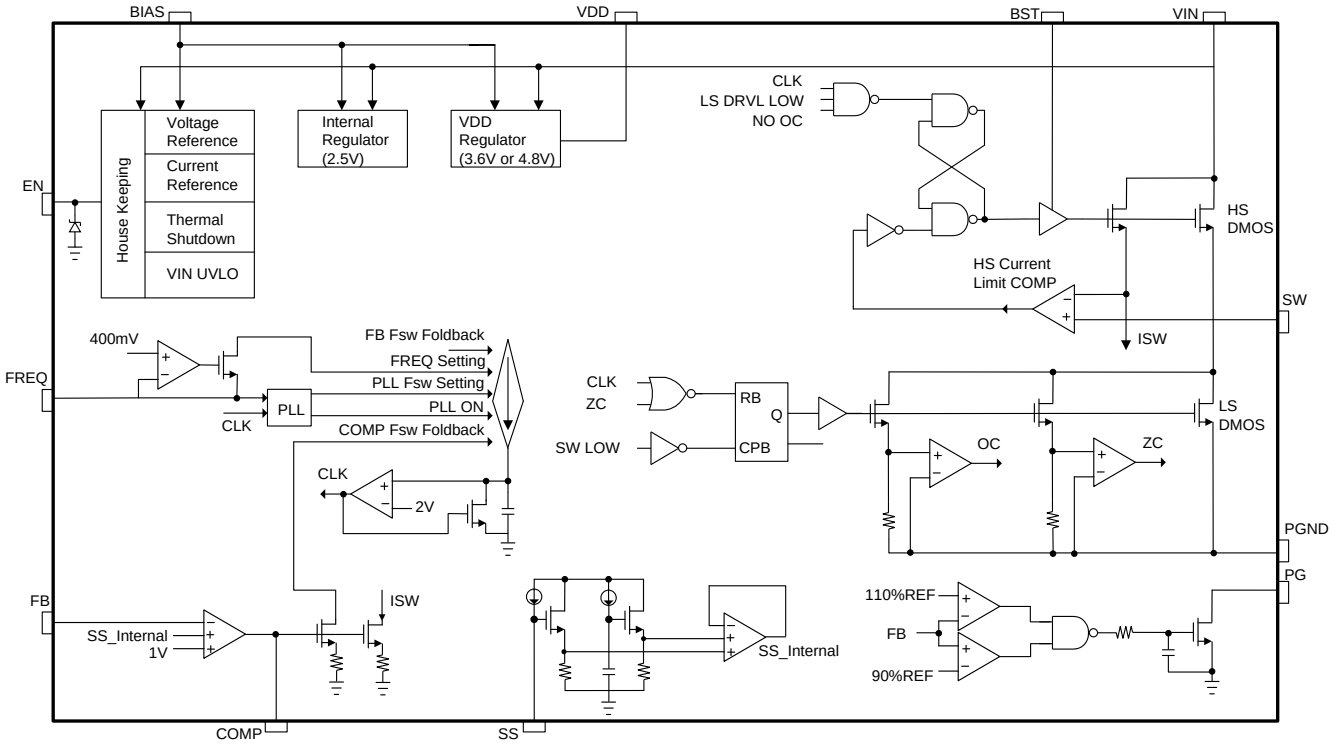


Figure 1: Functional Block Diagram

OPERATION

The MP4575 is a step-down switching regulator with integrated, high-voltage, power MOSFETs. The MP4575 features a wide input voltage range, high efficiency, external and internal soft start, programmable frequency, and comprehensive protection modes.

Pulse-Width Modulation (PWM) Control

The MP4575 uses peak-current-mode control to regulate the output voltage.

A PWM cycle is initiated by the internal clock at the beginning of every cycle. After the high-side MOSFET (HS-FET) turns on, the inductor current rises linearly to provide energy to the load. The HS-FET remains on until its current reaches the COMP voltage (V_{COMP}), which is the output of the internal error amplifier (EA). The output voltage of the EA depends on the difference of the output feedback voltage and the internal high-precision reference, and V_{COMP} decides how much energy should be transferred to the load. The higher the load current, the higher V_{COMP}. After the high-side switch is off, the low-side switch turns on, and the inductor current flows through the low-side switch. To prevent a shoot-through, a dead time is inserted to prevent the HS-FET and LS-FET from turning on at the same time. For each turn-on and turn-off in a switching cycle, the HS-FET remains on and off with a minimum on and off time limit.

Light-Load Operation

The MP4575 can achieve high efficiency during light load in two ways. First, when the load current decreases, the inductor current drops at same time. The LS-FET turns off to save driver loss when the inductor current drops to zero. Second, when the load decreases, the switching frequency is scaled down to reduce switching loss after V_{COMP} drops below a certain threshold.

Error Amplifier (EA)

The error amplifier (EA) compares the FB voltage with the internal reference and outputs a current proportional to the difference between the two. This current is used to charge the external compensation networks to form V_{COMP}, which is used to control the HS-FET peak current and regulate the output voltage.

Oscillator and SYNC Function

The internal oscillator frequency is set by a single external resistor (R_{FREQ}) connected between FREQ and GND. The frequency-setting resistor should be located close to the device. The relationship between the oscillator frequency and R_{FREQ} is shown in Table 1 on page 17.

During light load, the switching frequency is scaled down according to V_{COMP}. The switching frequency begins decreasing when V_{COMP} is below about 0.8V. Switching is disabled when V_{COMP} drops below about 0.7V.

To reduce switching loss and thermal dissipation, the switching frequency is decreased according to the FB voltage. When FB is lower than 25%xREF, the switching frequency starts to decrease from the normal value and drops to 5% of the normal value when FB is zero.

FREQ can be used to synchronize the internal oscillator rising edge to an external clock falling edge. Ensure that the high amplitude of the synchronous (SYNC) clock is higher than 1.5V and the low amplitude is lower than 1V to drive the internal logic. The recommended external SYNC frequency is in the range of 100kHz and 1MHz. There is no pulse width requirement, but there is always a parasitic capacitance of the pad. If the pulse width is too short, a clear rising and falling edge may not be seen due to the parasitic capacitance. A pulse longer than 100ns is recommended in application.

Enable (EN) Control

Enable (EN) is a control pin that turns the regulator on and off. Drive EN higher than 1.6V to turn on the regulator; drive EN lower than 1.3V to turn off the regulator. There is no internal pull-up or pull-down circuitry at EN, so when EN is floating, its status is uncertain.

EN is clamped internally using a 6.5V Zener diode between EN and GND. Connecting EN to a voltage source directly without any pull-up resistor requires limiting the voltage amplitude to ≤6V to prevent damage to the Zener diode. EN can be connected to a higher voltage (e.g.: VIN) through a pull-up resistor if the system

does not have another logic signal acting as the enable signal. Ensure that the pull-up resistor is high enough to ensure that the sink current going into EN is less than 150μA to avoid damaging the Zener diode. For example, when connecting EN to VIN = 12V, $R_{PULL-UP}$ ≥ (12V - 6.5V) ÷ 150μA = 37kΩ.

Soft Start (SS)

Soft start (SS) is implemented to ensure a smooth start-up of the output voltage during power-on and power-off. The soft start function also helps to reduce inrush current at start-up.

The soft start function is achieved by ramping SS up slowly and overriding the internal reference (REF) when SS - 900mV is lower than REF. When SS - 900mV is higher than REF, REF regains control. 900mV is the offset voltage of SS, which means that SS is detected as 0 internally when it is lower than 900mV. To minimize the delay for SS to reach 0.9V, an internal pull-up circuit with about 30μA of average current pulls SS up to 600mV first. Then use a 4μA constant current to charge SS until it reaches 2.5V. When SS is in the range of 0.9V to 1.9V, it overrides REF as the reference voltage of the error amplifier. During this period, the output voltage ramps up from 0 to the regulated value following SS rising. The soft-start time (t_{SS}) set by the external SS capacitor can be calculated with Equation (1):

$$t_{SS}(ms) = \frac{C_{SS}(nF) \times V_{REF}(V)}{I_{SS}(\mu A)} \quad (1)$$

Where C_{SS} is the external SS capacitor, V_{REF} is the internal reference voltage (1V), and I_{SS} is the 4μA SS charge current.

The delay time for SS reaching 900mV can be estimated with Equation (2):

$$t_{SS\_delay}(ms) = \frac{C_{SS}(nF) \times 0.6V}{30\mu A} + \frac{C_{SS}(nF) \times 0.3V}{4\mu A} \quad (2)$$

There is also an internal, fixed, 500μs soft start. The final SS time is determined by the longer time between 500μs and the external SS setting time.

When the output voltage is shorted to GND, the feedback voltage is pulled low, and then SS is discharged. The MP4575 soft starts again when the short at the output is removed.

Internal Regulator and BIAS

An internal 2.5V regulator powers all of the internal control circuits. This regulator uses VIN as the power supply when BIAS is lower than 3.2V and uses BIAS as the supply when BIAS is higher than 3.2V.

The VDD regulator powers the low-side driver and the BST regulator when the VDD voltage is higher than 4.5V. VDD is powered by V_{IN} when BIAS is floating and is regulated at 3.6V. When BIAS is higher than 4.2V, it powers VDD. VDD increases as BIAS rises with a 600mV voltage drop and is regulated at 4.8V when BIAS is higher than 5.4V. A 1μF decoupling capacitor is needed at VDD to make the capacitor as close to VDD as possible.

Using BIAS to power the internal regulator can improve efficiency. It is recommended to connect BIAS to an external power supply in the range of 3.3V to 5.5V. The output voltage is a good choice for this power supply if it is in above range. A 0.1μF to 1μF decoupling capacitor at BIAS is recommended.

Over-Voltage Protection (OVP)

The MP4575 monitors the feedback output voltage to achieve over-voltage protection (OVP). If the FB voltage is higher than 103%xREF, the MP4575 switches to sleep mode, the HS-FET turn offs, and the LS-FET turns on to discharge the output energy. The MP4575 returns to normal after the FB voltage drops below 103%xREF.

If the FB voltage is higher than 110%xREF, the HS-FET and LS-FET are turned off immediately. Both MOSFETs are latched, and the PG signal is asserted to indicate the fault status and if EN or VIN must be recycled to clear the protection.

Over-Current Protection (OCP)

The MP4575 has a cycle-by-cycle peak-current-limit protection and valley current detection protection. The inductor current is monitored during the HS-FET on state. If the inductor current exceeds the current limit value set by V_{COMP}, the HS-FET turns off immediately. Then, the LS-FET is turned on to discharge the energy, and the inductor current decreases. The HS-FET does not turn on again until the inductor valley current is below a certain current

threshold (valley current limit). This is useful for preventing an inductor current runaway. Both the peak current limit and the valley current limit values are dependent on the FB voltage. If the feedback output voltage is higher than 50%xREF, the current limit value is normal. If the feedback output voltage is lower than 50%xREF, the current limit decreases to half the normal value when the feedback output voltage is zero. This feature is useful for reducing OCP thermal dissipation, which may worsen when the output voltage is shorted. It is also useful for reducing high inrush current during start-up.

Under-Voltage Lockout (UVLO) Protection

The MP4575 has an input under-voltage lockout (UVLO) protection. When EN is active, the MP4575 is powered on when the input voltage is higher than the UVLO rising threshold, and is powered off when the input voltage drops below the UVLO falling threshold.

Thermal Shutdown Protection

The thermal shutdown is employed in the MP4575 by monitoring the IC temperature internally. If the junction temperature exceeds the threshold (typically 170°C), the regulator shuts off and turns on again when the temperature drops below 160°C. There is a hysteresis of about 10°C.

Power Good (PG)

The MP4575 uses one power good (PG) pin out to indicate normal operation after the soft-start time.

PG is the open drain of the internal MOSFET. PG should be connected to VDD or an external voltage source through a resistor (i.e.: 100kΩ). After the input voltage is applied, the MOSFET is turned on, and PG is pulled to GND before SS is ready. After the FB voltage reaches 90% of the REF voltage, the MOSFET turns off, and PG is pulled high by an external voltage source. When the FB voltage drops to 85% of the REF voltage, the PG voltage is pulled to GND to indicate a failure output status.

Floating Driver and Bootstrap Charging

An external bootstrap capacitor (typically 0.1μF) between BST and SW powers the floating power MOSFET driver. This floating driver has its own UVLO protection. This UVLO's rising threshold is 2.3V with a hysteresis of 300mV. The driver's UVLO is soft-start related. When the bootstrap voltage reaches its UVLO threshold, the soft-start circuit resets. When the bootstrap UVLO is removed, the soft-start reset is off, and the soft-start process resumes.

The dedicated internal bootstrap regulator regulates and charges the bootstrap capacitor to 4.2V. When the voltage between the BST and SW nodes is less than its regulation, a PMOS pass transistor from VIN to BST turns on. The charging current path is from VIN to BST to SW.

As long as VIN is sufficiently higher than V_{SW}, the bootstrap capacitor can be charged. When the HS-FET is on, VIN ≈ V_{SW}, so the bootstrap capacitor cannot be charged. When the LS-FET is on, the difference between VIN and V_{SW} is at its largest, making this the best period to charge. When there is no current in the inductor, V_{SW} = V_{OUT}, so the difference between VIN and V_{OUT} can charge the bootstrap capacitor.

At higher duty cycles, the time period available for bootstrap charging is shorter, so the bootstrap capacitor may not be sufficiently charged. If the internal circuit does not have sufficient voltage, and the bootstrap capacitor is not charged, extra external circuitry can be used to ensure that the bootstrap voltage is within the normal operating region.

APPLICATION INFORMATION

Setting the Switching Frequency

The MP4575 has an externally adjustable frequency. The switching frequency (f_{SW}) can be set using a resistor at FREQ (R_{FREQ}). Table 1 shows recommended R_{FREQ} values for various f_{SW} values. Refer to the f_{SW} vs. R_{FREQ} curve in the Typical Characteristics section on page 8 for more detailed values.

Table 1: f_{SW} vs. R_{FREQ}

f_{SW} (kHz)	R_{FREQ} (kΩ)
1000	47.5
900	56
800	63.4
700	73.2
600	84.5
500	102
400	133
300	178
200	261
100	523

Setting the Output Voltage

A resistive voltage divider from the output voltage to FB sets the output voltage. The voltage divider divides the output voltage down to the feedback voltage by the ratio shown in Equation (3):

$$V_{FB}=V_{OUT}\times\frac{R2}{R1+R2} \quad (3)$$

Calculated the output voltage with Equation (4):

$$V_{OUT}=V_{FB}\times\frac{R1+R2}{R2} \quad (4)$$

For example, if R1 is 10kΩ, then R2 can be calculated with Equation (5):

$$R2=\frac{10}{V_{OUT}-1}k\Omega \quad (5)$$

So for a 3.3V output voltage, R1 is 10kΩ, and R1 is 4.32kΩ.

Selecting the Inductor

The inductor provides a constant current to the output load while being driven by the switched input voltage. A larger-value inductor results in a lower ripple current and lower output ripple voltage, but also is physically larger, has a higher series resistance, and lower saturation current.

To determine the inductance, allow the inductor's peak-to-peak ripple current to equal approximately 30% of the maximum switch current limit. Ensure that the peak inductor current is less than the maximum switch current limit. The inductance value can be calculated with Equation (6):

$$L1=\frac{V_{OUT}}{f_{SW}\times\Delta I_L}\times\left(1-\frac{V_{OUT}}{V_{IN}}\right) \quad (6)$$

Where V_{OUT} is the output voltage, VIN is the input voltage, f_S is the switching frequency, and ΔI_L is the peak-to-peak inductor ripple current.

Choose an inductor that will not saturate under the maximum inductor peak current. The peak inductor current can be calculated with Equation (7):

$$I_{LP}=I_{LOAD}+\frac{V_{OUT}}{2\times f_{SW}\times L1}\times\left(1-\frac{V_{OUT}}{V_{IN}}\right) \quad (7)$$

Where I_{LOAD} is the load current.

Selecting the Input Capacitor

The input current to the step-down converter is discontinuous and requires a capacitor to supply AC current to the step-down converter while maintaining the DC input voltage. Use capacitors with low equivalent series resistances (ESR) for the best performance. Ceramic capacitors are preferred, but tantalum or low-ESR electrolytic capacitors may also be sufficient.

For simplification, choose an input capacitor with an RMS current rating greater than half of the maximum load current. The input capacitor (C1) can be electrolytic, tantalum, or ceramic.

When using electrolytic or tantalum capacitors, place a small, high-quality, ceramic capacitor (0.1μF) as close to the IC as possible. When using ceramic capacitors, ensure that they have enough capacitance to provide a sufficient charge to prevent excessive voltage ripple at the input. The input voltage ripple caused by capacitance can be approximated with Equation (8):

$$\Delta V_{IN} = \frac{I_{LOAD}}{f_{SW} \times C1} \times \frac{V_{OUT}}{V_{IN}} \times \left(1 - \frac{V_{OUT}}{V_{IN}}\right) \quad (8)$$

Selecting the Output Capacitor

The output capacitor (C2) maintains the DC output voltage. Use ceramic, tantalum, or low-ESR electrolytic capacitors. Low ESR capacitors are recommended to keep the output voltage ripple low. The output voltage ripple can be estimated with Equation (9):

$$\Delta V_{OUT} = \frac{V_{OUT}}{f_{SW} \times L} \times \left(1 - \frac{V_{OUT}}{V_{IN}}\right) \times \left(R_{ESR} + \frac{1}{8 \times f_{SW} \times C2}\right) (9)$$

Where L is the inductor value, and R_{ESR} is the ESR value of the output capacitor.

For ceramic capacitors, the capacitance dominates the impedance at the switching frequency and contributes the most to the output voltage ripple. For simplification, the output voltage ripple can be estimated with Equation (10):

$$\Delta V_{OUT} = \frac{V_{OUT}}{8 \times f_{SW}^2 \times L \times C2} \times \left(1 - \frac{V_{OUT}}{V_{IN}}\right) \quad (10)$$

For tantalum or electrolytic capacitors, the ESR dominates the impedance at the switching frequency. For simplification, the output ripple can be approximated with Equation (11):

$$\Delta V_{OUT} = \frac{V_{OUT}}{f_{SW} \times L} \times \left(1 - \frac{V_{OUT}}{V_{IN}}\right) \times R_{ESR} \quad (11)$$

The characteristics of the output capacitor also affect the stability of the regulation system. The MP4575 can be optimized for a wide range of capacitances and ESR values.

Compensation Components

The MP4575 employs current-mode control for easy compensation and fast transient response. COMP is the output of the internal error amplifier and controls system stability and transient response. A series resistor-capacitor combination sets a pole-zero combination to control the control system's characteristics. The DC gain of the voltage feedback loop can be calculated with Equation (12):

$$A_{VDC} = R_{LOAD} \times G_{CS} \times A_{VEA} \times \frac{V_{FB}}{V_{OUT}} \quad (12)$$

Where A_{VEA} is the error amplifier voltage gain (1000V/V), G_{CS} is the current-sense transconductance (12A/V), and R_{LOAD} is the load resistor value.

The system has two important poles: one from the compensation capacitor (C3) and the output resistor of error amplifier, and the other due to the output capacitor and the load resistor. These poles can be determined with Equation (13) and Equation (14):

$$f_{P1} = \frac{G_{EA}}{2\pi \times C3 \times A_{VEA}} \quad (13)$$

$$f_{P2} = \frac{1}{2\pi \times C2 \times R_{LOAD}} \quad (14)$$

Where G_{EA} is the error-amplifier transconductance (540μA/V).

The system has one important zero due to the compensation capacitor and the compensation resistor (R3). This zero can be determined with Equation (15):

$$f_{Z1} = \frac{1}{2\pi \times C3 \times R3} \quad (15)$$

The system may have another significant zero if the output capacitor has a large capacitance or a high ESR value. This zero can be determined with Equation (16):

$$f_{ESR} = \frac{1}{2\pi \times C2 \times R_{ESR}} \quad (16)$$

In this case, a third pole set by the compensation capacitor (C4) and the compensation resistor can compensate for the effect of the ESR zero. This pole can be determined with Equation (17):

$$f_{P3} = \frac{1}{2\pi \times C4 \times R3} \quad (17)$$

The goal of compensation design is to shape the converter transfer function for a desired loop gain. The system crossover frequency where the feedback loop has unity gain is important, since lower crossover frequencies result in slower line and load transient responses, while higher crossover frequencies lead to system instability. Generally, set the crossover frequency to ~0.1xf_{SW}.

Use the following steps to design the compensation:

1. Choose R3 to set the desired crossover frequency. R3 can be determined with Equation (18):

$$R3 = \frac{2\pi \times C2 \times f_C}{G_{EA} \times G_{CS}} \times \frac{V_{OUT}}{V_{FB}} \quad (18)$$

   Where f_C is the desired crossover frequency.

2. Choose C3 to achieve the desired phase margin. For applications with typical inductor values, set the compensation zero (f_{Z1}) to <0.25xf_C to provide a sufficient phase margin. C3 can be calculated with Equation (19):

$$C3 > \frac{4}{2\pi \times R3 \times f_C} \quad (19)$$

3. Determine if C4 is required. C4 is required if the ESR zero of the output capacitor is located at <0.5xf_{SW}, or Equation (20) is valid:

$$\frac{1}{2\pi \times C2 \times R_{ESR}} < \frac{f_{SW}}{2} \quad (20)$$

   If this is the case, use C4 to set the pole (f_{P3}) at the location of the ESR zero. Determine C4 with Equation (21):

$$C4 = \frac{C2 \times R_{ESR}}{R3} \quad (21)$$

External Bootstrap Diode

For high duty-cycle operations where V_{OUT}/VIN > 65%, the time period available to the bootstrap charging is less, so the bootstrap capacitor may not be charged sufficiently. This affects efficiency and normal operation. An external bootstrap diode from the 3V - 5V rail to BST can help charge the bootstrap capacitor and enhance efficiency (see Figure 2). The output voltage is a good choice for this power supply if it is in above range. The bootstrap diode can be a low-cost one such as IN4148 or BAT54.

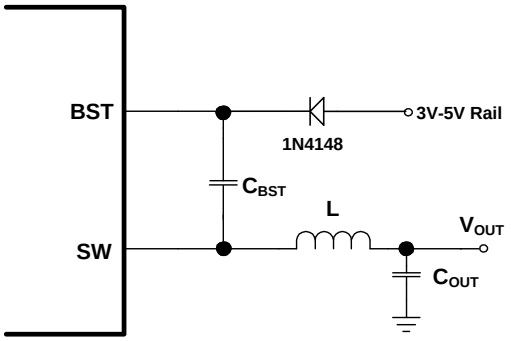


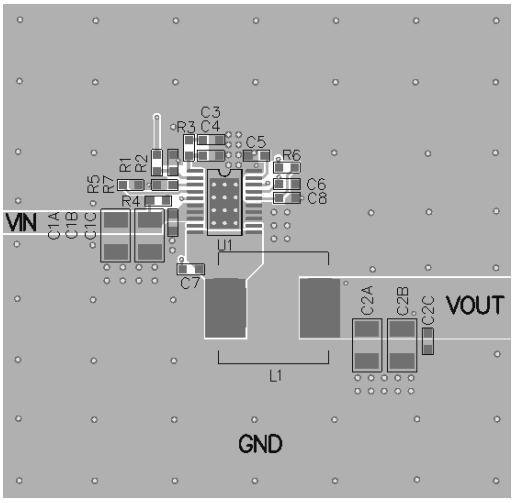
Figure 2: External Bootstrap Diode

At no load or light load, the converter may operate in pulse-skipping mode to maintain the output-voltage regulation. Under this condition, V_{SW} = V_{OUT} for most of the time, so the diode from V_{OUT} to BST cannot charge the bootstrap capacitor. For a sufficient gate voltage during pulse-skipping mode, VIN - V_{OUT} should be no less than 3V. For example, if V_{OUT} = 3.3V, then VIN must exceed 3.3V + 3V = 6.3V to maintain a sufficient bootstrap voltage at no load or light load. To meet this requirement, EN can program the input UVLO voltage to V_{OUT} + 3V.

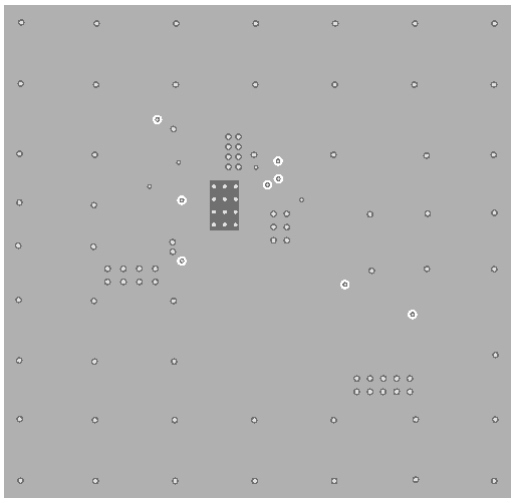
PCB Layout Guidelines

Efficient PCB layout is critical for stable operation. For best results, refer to Figure 3 and follow the guidelines below.

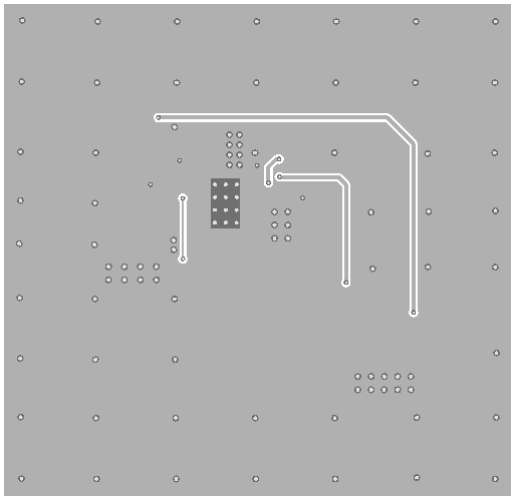
1. Place the ceramic input capacitor, especially the small package size (0603) input bypass capacitor, as close to IN and GND as possible.
2. Keep the connection of the input capacitor and VIN as short and wide as possible.
3. Place the VDD capacitor to VDD and GND as close as possible.
4. Use a large ground plane to directly connect to GND.
5. Add vias near GND if the bottom layer is a ground plane.
6. Route SW and BST away from sensitive analog areas such as FB.
7. Ensure that all feedback connections are short and direct.
8. Place the feedback resistors as close to the chip as possible.
9. Connect VIN, SW, and especially GND and the exposed pad to large copper areas to cool the chip for improved thermal performance and long-term reliability.



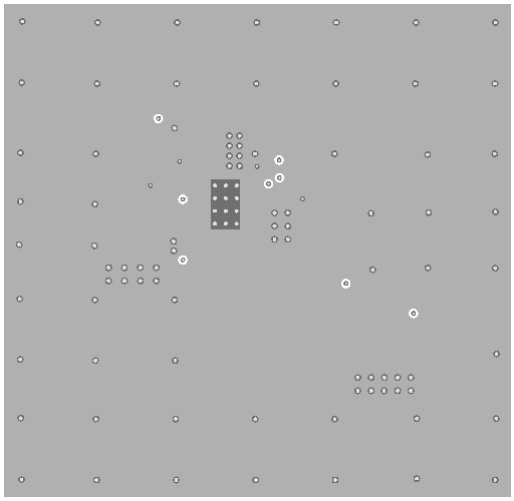
Top Layer



Inner Layer 1



Inner Layer 2



Bottom Layer

Figure 3: Recommended PCB Layout

TYPICAL APPLICATION CIRCUIT

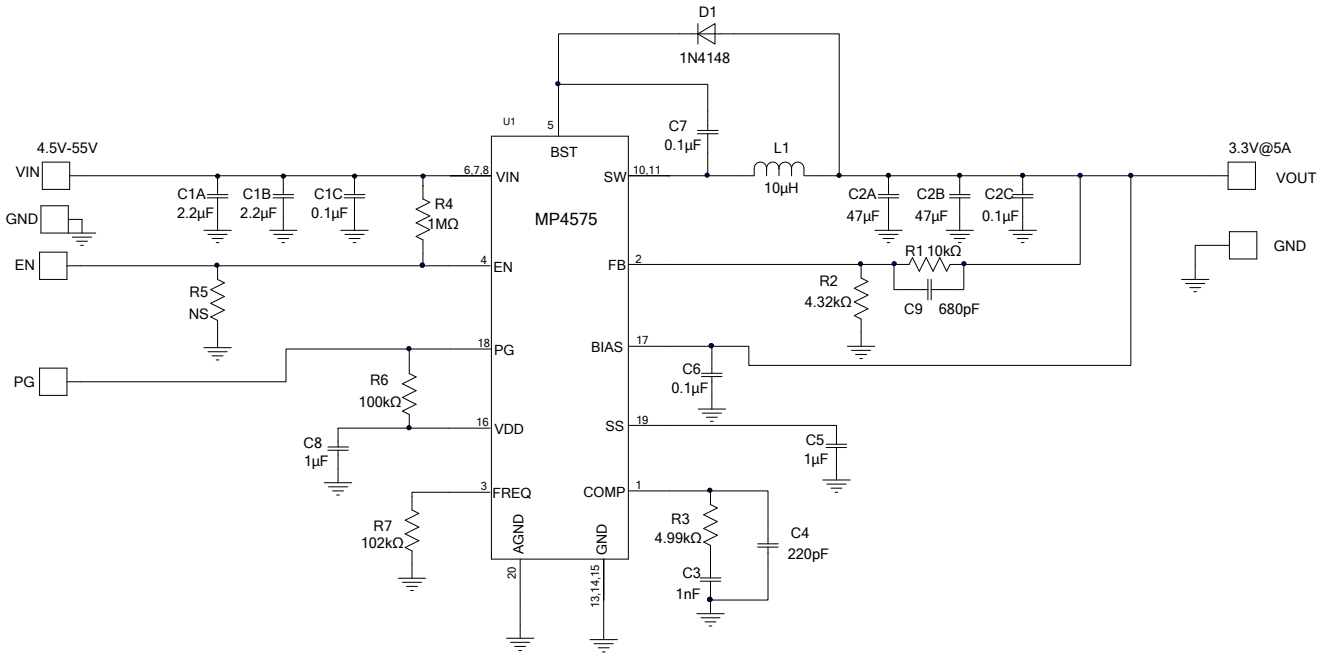
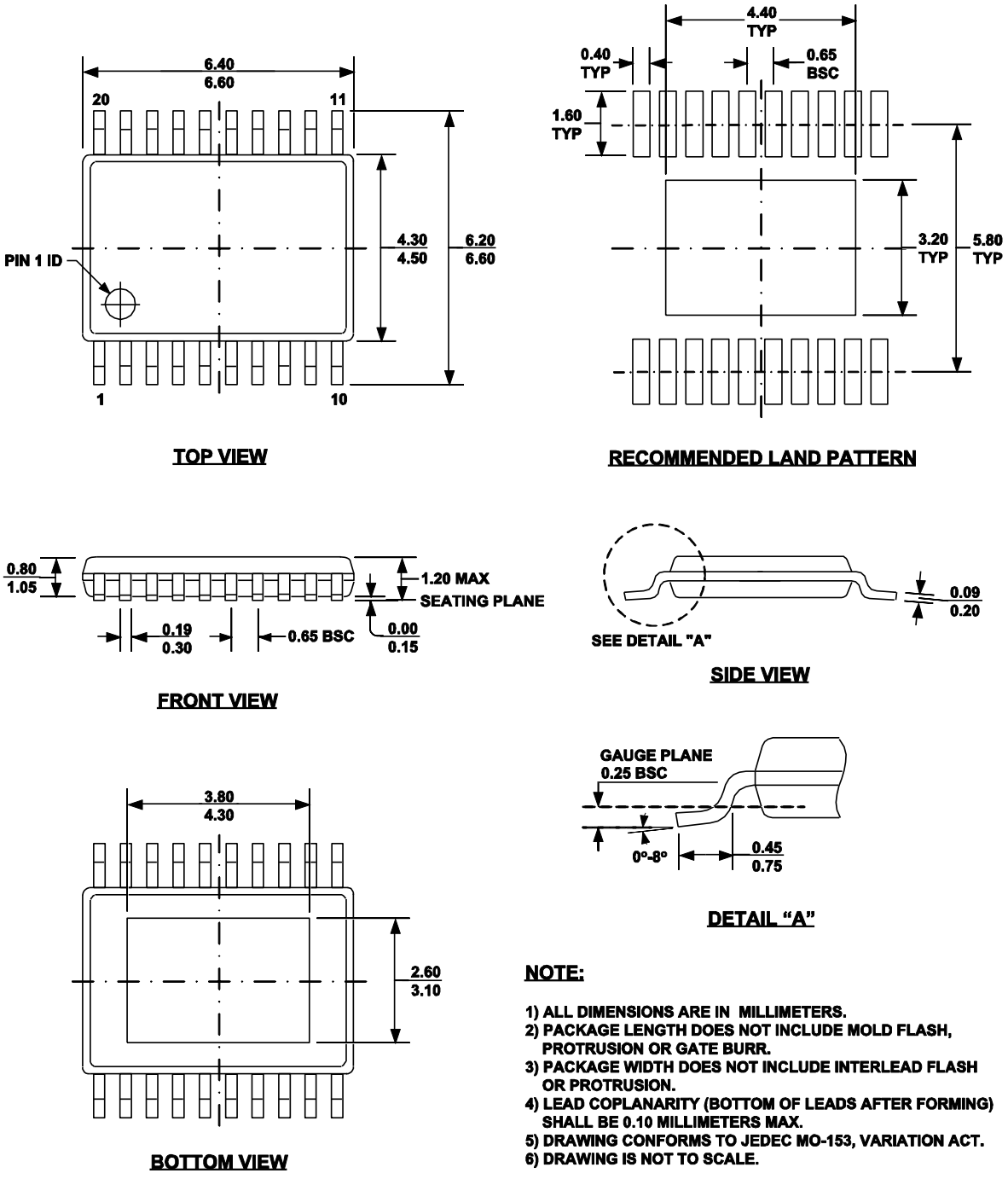


Figure 4: 3.3V Output Typical Application Circuit

PACKAGE INFORMATION

TSSOP-20 EP
(Exposed Pad)



NOTE:

1) ALL DIMENSIONS ARE IN MILLIMETERS.
2) PACKAGE LENGTH DOES NOT INCLUDE MOLD FLASH, PROTRUSION OR GATE BURR.
3) PACKAGE WIDTH DOES NOT INCLUDE INTERLEAD FLASH OR PROTRUSION.
4) LEAD COPLANARITY (BOTTOM OF LEADS AFTER FORMING) SHALL BE 0.10 MILLIMETERS MAX.
5) DRAWING CONFORMS TO JEDEC MO-153, VARIATION ACT.
6) DRAWING IS NOT TO SCALE.

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Телефон: 8 (812) 309-75-97 (многоканальный)
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Электронная почта: ocean@oceanchips.ru
Web: http://oceanchips.ru/
Адрес: 198099, г. Санкт-Петербург, ул. Калинина, д. 2, корп. 4, лит. А