MCP795WXX/MCP795BXX

SPI Real-Time Clock Calendar with Enhanced Features and Battery Switchover

Device Selection Table

Part Number	32 kHz Boot-up	SRAM (Bytes)	EEPROM (Kbits)	Unique ID
MCP795W20	No	64	2	Blank
MCP795W10	No	64	1	Blank
MCP795W21	No	64	2	EUI-48™
MCP795W11	No	64	1	EUI-48™
MCP795W22	No	64	2	EUI-64™
MCP795W12	No	64	1	EUI-64™
MCP795B20	Yes	64	2	Blank
MCP795B10	Yes	64	1	Blank
MCP795B21	Yes	64	2	EUI-48™
MCP795B11	Yes	64	1	EUI-48™
MCP795B22	Yes	64	2	EUI-64™
MCP795B12	Yes	64	1	EUI-64™
Note: Watchdog Timer and Event Detects in all devices.				

Timekeeping Features:

- Real-Time Clock/Calendar:
  - Hours, Minutes, Seconds, Hundredth of Seconds, Day of Week, Month, Year, Leap Year
- Crystal Oscillator requires External 32,768 kHz Tuning Fork Crystal and Load Capacitors.
- Clock Out Function:
  - 1Hz, 4.096 kHz, 8.192 kHz, 32.768 kHz
- 32 kHz Boot-up Clock at Power-up (MCP795BXX)
- 2 Programmable Alarms – Supports $\overline{\text{IRQ}}$ or $\overline{\text{WDO}}$
- Programmable open drain output – Alarm or Interrupt
- On-Chip Digital Trimming/Calibration:
  - +/- 255 PPM range in 1 PPM steps
- Power-Fail Time-Stamp @ Battery Switchover:
  - Logs time when VCC fails and VCC is restored

Low-Power Features:

- Wide Operating Voltage:
  - VCC: 1.8V to 5.5V
  - VBAT: 1.3V to 5.5V
- Low Operating Current:
  - VCC Standby Current < 1uA @ 3V
  - VBAT Timekeeping Current: <700nA @ 1.8V
- Automatic Battery Switchover from VCC to VBAT:
  - Backup power for timekeeping and SRAM retention

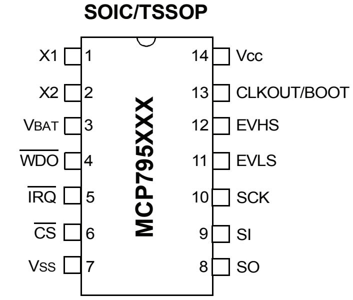
User Memory:

- 64-Byte Battery-Backed SRAM
- 2 Kbit and 1 Kbit EEPROM Memory:
  - Software block write-protect (¼, ½, or entire array)
  - Write Page mode (up to 8 bytes)
  - Endurance: 1M erase/write cycles
- 128-Bit Unique ID in Protected Area of EEPROM:
  - Available blank or preprogrammed
  - EUI-48™ or EUI-64™ MAC address
  - Unlock sequence for user programming

Enhanced Features:

- SPI Clock Speed up to 10 MHz
- Programmable Watchdog Timer:
  - Dedicated watchdog output pin
  - Dual retrigger using SPI bus or EVHS digital input
- Dual Configurable Event Detect Inputs:
  - High-Speed Digital Event Detect (EVHS) with pulse count for 1st, 4th,16th or 32nd event
  - Low-Speed Event Detect (EVLS) with programmable debounce delays of 31 msec and 500 msec
  - Edge triggered (rising or falling)
  - Operates from VCC or VBAT
- Operating Temperature Ranges:
  - Industrial (I Temp): -40°C to +85°C.
- Packages include 14-Lead SOIC and TSSOP

SOIC/TSSOP



Note: MCP795XXX is used in this document as a generic part number for the MCP795WXX, MCP795BXX devices.

Description:

The MCP795XXX is a low-power Real-Time Clock/ Calendar (RTCC) that uses digital trimming compensation for an accurate clock/calendar, an interrupt output to support alarms and events, a power sense circuit that automatically switches to the backup supply, non-volatile memory for safe data storage and several enhanced features that support system requirements.

Along with a low-cost 32,768 kHz crystal, this RTCC tracks time using several internal registers and then communicates the data over a 10 MHz SPI bus that is fast enough to support a programmable millisecond alarm.

The device is fully accessible through the serial interface, while VCC is between 1.8V and 5.5V, but can operate down to 1.3V through the backup supply connected to the VBAT input for timekeeping and SRAM retention only.

As part of the power sense circuit, a time saver function is implemented to store the time when main power is lost and again, when power is restored to log the duration of a power failure.

Along with the onboard serial EEPROM and battery-backed SRAM, a 128-bit protected space is available for a unique ID. This space can be ordered preprogrammed with a MAC address, or blank for the user to program.

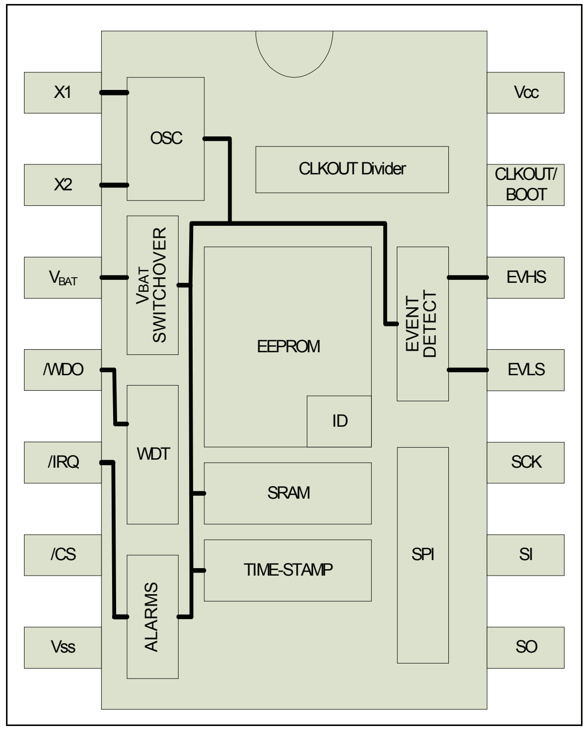
This clock/calendar automatically adjusts for months with fewer than 31 days including corrections for leap years. The clock operates in either 24-hour or 12-hour format with AM/PM indicator and settable alarm(s).

Using the external crystal, the CLKOUT pin can be set to generate a number of output frequencies. In addition, the MCP795BXX devices support a 32 kHz clock output at power-up on the CLKOUT/BOOT pin by using the same crystal driving the RTCC device.

For versatility, a digital event detect with a programmable pulse count can identify the 1st, 4th, 16th or 32nd pulse before sending an interrupt. A second event detect with built-in debounce input filter was also implemented to support noisy mechanical switches.

Since many microcontrollers do not have an integrated Watchdog Timer, this peripheral has been implemented in the RTCC. For many applications, this function must be performed outside the microcontroller for increased robustness.

FIGURE 1-1: BLOCK DIAGRAM



 Preliminary

1.0 ELECTRICAL CHARACTERISTICS

Absolute Maximum Ratings (†)

VCC..6.5V
All inputs and outputs w.r.t. VSS .... -0.6V to +6.5V
Storage temperature ....-65°C to +150°C
Ambient temperature under bias...-40°C to +85°C
ESD protection on all pins...4 kV

† NOTICE: Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at those or any other conditions above those indicated in the operational listings of this specification is not implied. Exposure to maximum rating conditions for extended periods may affect device reliability.

TABLE 1-1: DC CHARACTERISTICS

DC CHARACTERISTICS			Industrial (I): TAMB = -40°C to +85°C VCC = 1.8V to 5.5V			
Param. No.	**Sym.**	**Characteristic**	**Min.**	**Max.**	**Units**	**Test Conditions**
D001	VIH1	High-level input voltage	.7 VCC	VCC+1	V	
D002	VIL1	Low-level input voltage	-0.3	0.3VCC	V	VCC ≥ 2.5V
D003	VIL2		-0.3	0.2VCC	V	VCC < 2.5V
D004	VOL	Low-level output voltage	—	0.4	V	IOL = 2.1 mA
D005	VOL		—	0.2	V	IOL = 1.0 mA, VCC < 2.5V
D006	VOH	High-level output voltage	VCC -0.5	—	V	IOH = -400 µA
D007	ILI	Input leakage current		±1	µA	$\overline{CS}$ = VCC, VIN = VSS TO VCC
D008	ILO	Output leakage current		±1	µA	$\overline{CS}$ = VCC, VOUT = VSS TO VCC
D009	CINT	Internal Capacitance (all inputs and outputs)	—	7	pF	TAMB = 25°C, CLK = 1.0 MHz VCC = 5.0V (Note 1)
D010	ICC Read	Operating Current	—	3	mA	VCC = 5.5V; FCLK = 10.0 MHz SO = Open
D011	IDD write	Write Current	—	5	mA	VCC = 5.5V
D012	IBAT	VBAT Current	—	700	nA	VBAT = 1.8V @ 25°C (Note 2)
D013	VTRIP	VBAT Change Over	1.3	1.7	V	1.5V typical at TAMB = 25°C
D014	VCCFT	VCC Fall Time	300		µs	From VTRIP (max) to VTRIP (min)
D015	VCCRT	VCC Rise Time	0		µs	From VTRIP (min) to VTRIP (max)
D016	VBAT	VBAT Voltage Range	1.3	5.5	V	—
D017	ICCS	Standby Current	—	1	µA	—

Note 1: This parameter is periodically sampled and not 100% tested.
2: With oscillator running.

TABLE 1-2: AC CHARACTERISTICS

AC CHARACTERISTICS			Industrial (I): TAMB = -40°C to +85°C VCC = 1.8V to 5.5V			
Param. No.	**Sym.**	**Characteristic**	**Min.**	**Max.**	**Units**	**Test Conditions**
1	FCLK	Clock Frequency	— — —	10 5 3	MHz MHz MHz	4.5V ≤ Vcc ≤ 5.5V 2.5V ≤ Vcc < 4.5V 1.8V ≤ Vcc < 2.5V
2	TCSS	$\overline{CS}$ Setup Time	50 100 150	— — —	ns ns ns	4.5V ≤ Vcc ≤ 5.5V 2.5V ≤ Vcc < 4.5V 1.8V ≤ Vcc < 2.5V
3	TCSH	$\overline{CS}$ Hold Time	50 100 150	— — —	ns ns ns	4.5V ≤ Vcc ≤ 5.5V 2.5V ≤ Vcc < 4.5V 1.8V ≤ Vcc < 2.5V
4	TCSD	$\overline{CS}$ Disable Time	50	—	ns	—
5	TSU	Data Setup Time	10 20 30	— — —	ns ns ns	4.5V ≤ Vcc ≤ 5.5V 2.5V ≤ Vcc < 4.5V 1.8V ≤ Vcc < 2.5V
6	THD	Data Hold Time	20 40 50	— — —	ns ns ns	4.5V ≤ Vcc ≤ 5.5V 2.5V ≤ Vcc < 4.5V 1.8V ≤ Vcc < 2.5V
7	TR	CLK Rise Time	—	100	ns	(Note 1)
8	TF	CLK Fall Time	—	100	ns	(Note 1)
9	THI	Clock High Time	50 100 150	— — —	ns ns ns	4.5V ≤ Vcc ≤ 5.5V 2.5V ≤ Vcc < 4.5V 1.8V ≤ Vcc < 2.5V
10	TLO	Clock Low Time	50 100 150	— — —	ns ns ns	4.5V ≤ Vcc ≤ 5.5V 2.5V ≤ Vcc < 4.5V 1.8V ≤ Vcc < 2.5V
11	TCLD	Clock Delay Time	50	—	ns	—
12	TCLE	Clock Enable Time	50	—	ns	—
13	TV	Output Valid from Clock Low	— — —	50 100 160	ns ns ns	4.5V ≤ Vcc ≤ 5.5V 2.5V ≤ Vcc < 4.5V 1.8V ≤ Vcc < 2.5V
14	THO	Output Hold Time	0	—	ns	(Note 1)
15	TDIS	Output Disable Time	— — —	40 80 160	ns ns ns	4.5V ≤ Vcc ≤ 5.5V (Note 1) 2.5V ≤ Vcc < 4.5V (Note 1) 1.8V ≤ Vcc < 2.5V (Note 1)
16	TWC	Internal Write Cycle Time	—	5	ms	(Note 3)
17	—	Endurance	1,000,000	—	E/W Cycles	(Note 2)

Note 1: This parameter is periodically sampled and not 100% tested.

2: This parameter is not tested but ensured by characterization. For endurance estimates in a specific application, please consult the Total Endurance™ Model which can be obtained from Microchip's web site: www.microchip.com.

3: TWC begins on the rising edge of $\overline{CS}$ after a valid write sequence and ends when the internal write cycle is complete.

FIGURE 1-1: SERIAL INPUT TIMING

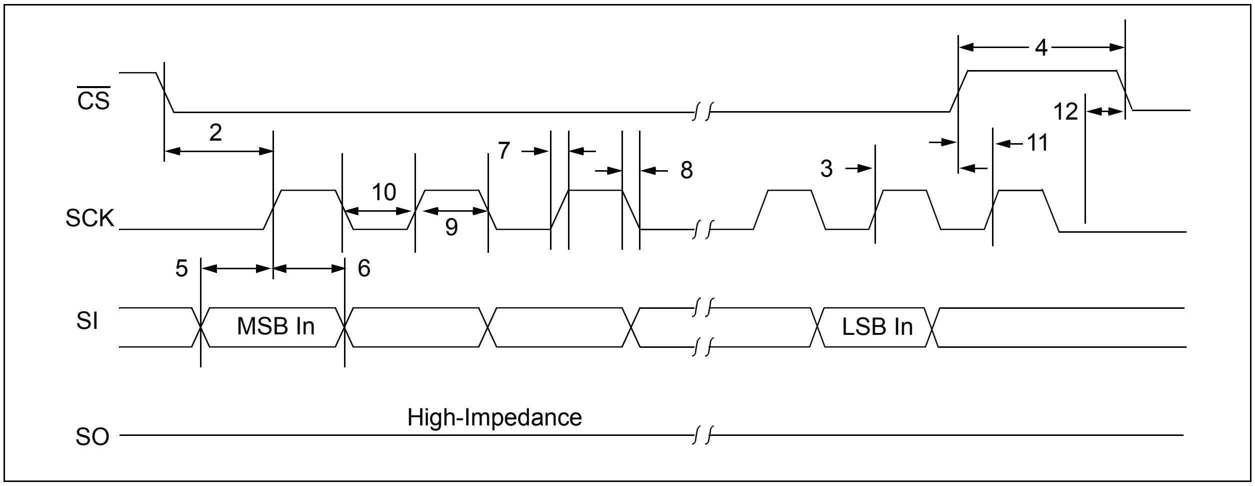
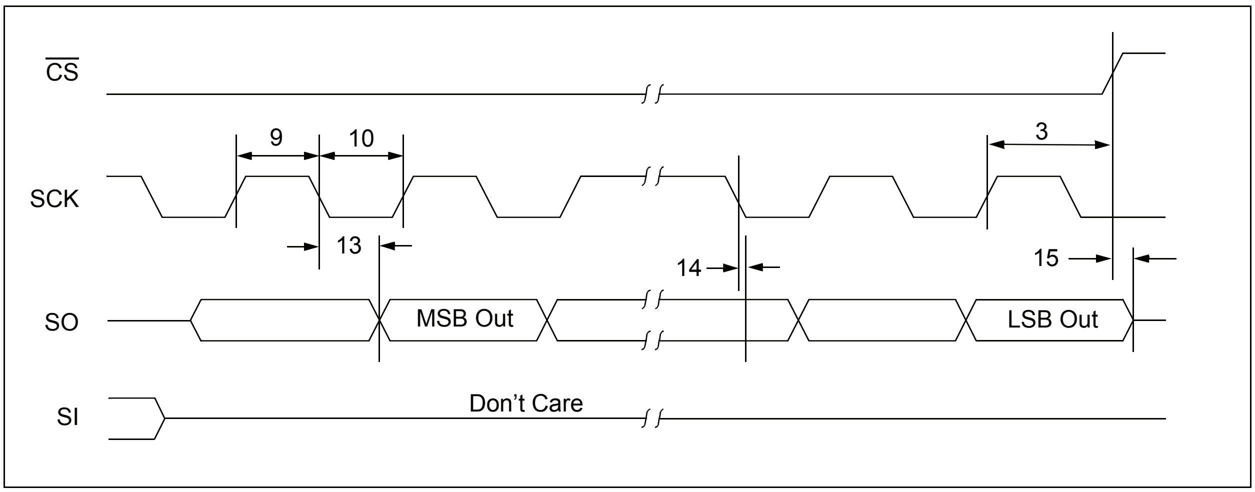


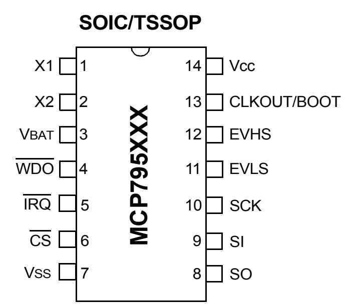
FIGURE 1-2: SERIAL OUTPUT TIMING



2.0 PIN DESCRIPTION

The descriptions of the pins are listed in Table 2-1.

FIGURE 2-1: DEVICE PINOUTS



2.1 Chip Select ($\overline{CS}$)

A low level on this pin selects the device. A high level deselects the device and forces it into Standby mode. However, a programming cycle which is already initiated or in progress will be completed, regardless of the $\overline{CS}$ input signal. If $\overline{CS}$ is brought high during a program cycle, the device will go in Standby mode as soon as the programming cycle is complete. When the device is deselected, SO goes into the high-impedance state, allowing multiple parts to share the same SPI bus. A low-to-high transition on $\overline{CS}$ after a valid write sequence initiates an internal write cycle. After power-up, a low level on $\overline{CS}$ is required prior to any sequence being initiated.

2.2 Serial Output (SO)

The SO pin is used to transfer data out of the MCP795XXX. During a read cycle, data is shifted out on this pin after the falling edge of the serial clock.

2.3 Watchdog Output ($\overline{WDO}$)

This pin is a hardware open drain from the internal watchdog circuit. This pin requires an external pull-up to VCC. When a watchdog overflow occurs the onboard N-Channel will pulse this pin low. The pulse duration is user selectable (Address 0x0A:4). This pin has a maximum sink current of 10mA.

2.4 Serial Input (SI)

The SI pin is used to transfer data into the device. It receives instructions, addresses and data. Data is latched on the rising edge of the serial clock.

2.5 Serial Clock (SCK)

The SCK is used to synchronize the communication between a master and the MCP795XXX. Instructions, addresses or data present on the SI pin are latched on the rising edge of the clock input, while data on the SO pin is updated after the falling edge of the clock input.

2.6 Interrupt Output ($\overline{IRQ}$)

The $\overline{IRQ}$ pin is shared with the onboard event detect and the Alarms. This pin requires an external pull-up to VCC or VBAT. The onboard N-Channel will pull the pin low during an event detection or an alarm. The pin remains low until such time that the interrupt flag in the register is cleared by software. This pin has a maximum sink current of 10mA.

2.7 X1, X2

The X1 and X2 pins connect to the onboard oscillator block. X1 is the input to the module and X2 is the output of the module. The device can be run from an external CMOS signal by feeding into the X1 pin. If driving X1 the X2 pin should be a No Connect.

2.8 VBAT

The VBAT pin is a secondary supply input to maintain the Clock and SRAM contents when VCC is removed.

2.9 CLKOUT/BOOT

The CLKOUT is a push-pull output that can be used to generate a squarewave or is used for the boot-up clock output at power-up. Please refer to **Section 9.1.2, Clockout Function** for more details.

2.10 EVHS and EVLS

The EVHS and EVLS are inputs for the High and Low Speed Event Detection circuit.

TABLE 2-1: PIN DESCRIPTIONS

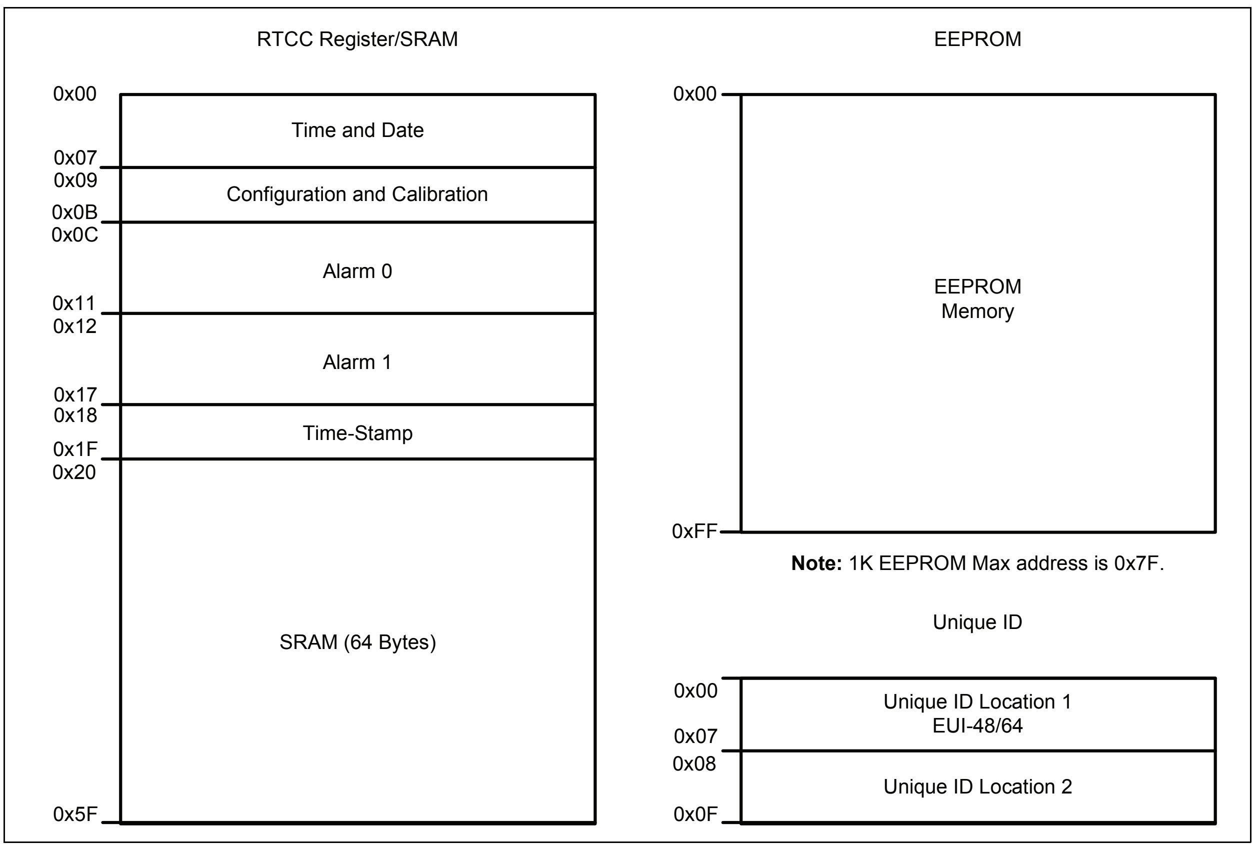
Pin Name	Pin Function
VSS	Ground
X1	Xtal Input, External Oscillator Input
X2	Xtal Output
VBAT	Battery Backup Input (3V Typ)
VCC	+1.8V to +5.5V Power Supply
SI	Serial Input
$\overline{WDO}$	Watchdog Output
SCK	Serial Clock
CLKOUT/ BOOT	Clock Out (Boot Clock on MCP795BXX)
$\overline{CS}$	Chip Select
$\overline{IRQ}$	Interrupt Ouput
EVHS	High-Speed Event Detect Input
EVLS	Low-Speed Event Detect Input
SO	Serial Output

2.11 RTCC Memory Map

The RTCC registers are contained in addresses 0x00h-0x1fh. 64 bytes of user-accessable SRAM are located in the address range 0x20-0x5f. The SRAM memory is a separate block from the RTCC control and Configuration registers. All SRAM locations are battery-backed-up during a VCC power fail. Unused locations are not accessible.

- Addresses 0x00h-0x07h are the RTCC Time and Date registers. These are read/write registers. Care must be taken when writing to these registers with the oscillator running.
- Incorrect data can appear in the Time and Date registers if a write is attempted during the time frame where these internal registers are being incremented. The user can minimize the likelihood of data corruption by ensuring that any writes to the Time and Date registers occur before the contents of the second register reach a value of 0x59H.
- Addresses 0x08h-0x0Bh are the device Configuration, Calibration, Watchdog Configuration and Event Detect Configuration registers.
- Addresses 0x0ch-0x11h are the Alarm 0 registers. These are used to set up the Alarm 0, the interrupt pin and the Alarm 0 compare.
- Addresses 0x12h-0x17h are the Alarm 1 registers. These are used to set up the Alarm 1, the interrupt pin and the Alarm 1 compare, Alarm 1 offers a enhanced resolution of tenth and hundredths of seconds.
- Addresses 0x18h-0x1Fh are used for the Power-Down and Power-Up time-stamp feature. The detailed memory map is shown in Table 4-1. No error checking is provided when loading Time and Date registers.

FIGURE 2-2: MEMORY MAP



3.0 SPI BUS OPERATION

The MCP795XXX is designed to interface directly with the Serial Peripheral Interface (SPI) port of many of today's popular microcontroller families, including Microchip's PIC® microcontrollers. It may also interface with microcontrollers that do not have a built-in SPI port by using discrete I/O lines programmed properly in software to match the SPI protocol.

The MCP795XXX contains an 8-bit instruction register.

The device is accessed via the SI pin, with data being clocked in on the rising edge of SCK. The CS pin must be low for the entire operation.

Table 3-1 contains a list of the possible instruction bytes and format for device operation. All instructions, addresses, and data are transferred MSb first, LSb last.

Data (SI) is sampled on the first rising edge of SCK after CS goes low.

TABLE 3-1: INSTRUCTION SET SUMMARY

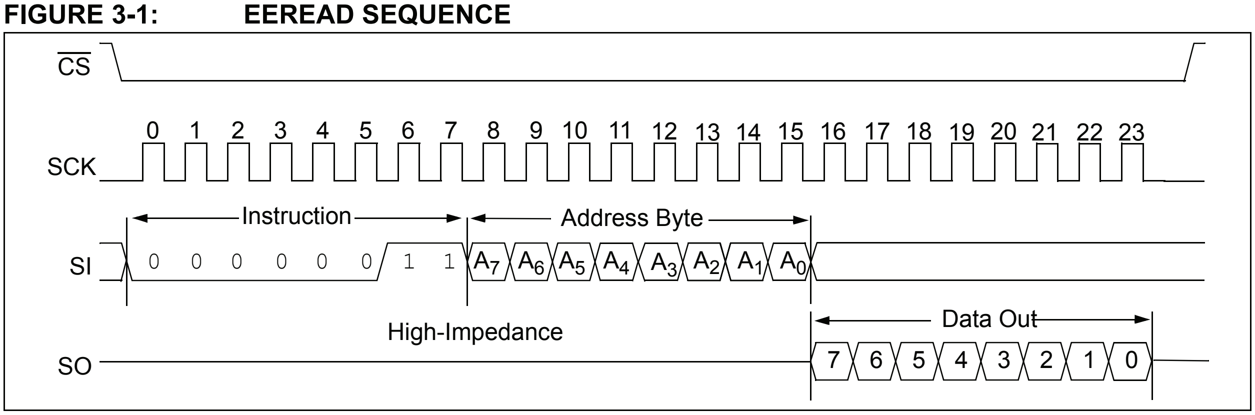
Instruction Name	Instruction Format	Description
EEREAD	0000 0011	Read data from EE memory array beginning at selected address
EEWRITE	0000 0010	Write data to EE memory array beginning at selected address
EEWRDI	0000 0100	Reset the write enable latch (disable write operations)
EEWREN	0000 0110	Set the write enable latch (enable write operations)
SRREAD	0000 0101	Read STATUS register
SRWRITE	0000 0001	Write STATUS register
READ	0001 0011	Read RTCC/SRAM array beginning at selected address
WRITE	0001 0010	Write RTCC/SRAM data to memory array beginning at selected address
UNLOCK	0001 0100	Unlock ID Locations
IDWRITE	0011 0010	Write to the ID Locations
IDREAD	0011 0011	Read the ID Locations
CLRWDT	0100 0100	Clear Watchdog TImer
CLRRAM	0101 0100	Clear RAM Location to '0'

3.1 Read Sequence

The device is selected by pulling CS low. The various 8-bit read instructions are transmitted to the MCP795XXX followed by an 8-bit address. See Figure 3-1 for more details.

After the correct instruction and address are sent, the data stored in the memory at the selected address is shifted out on the SO pin. Data stored in the memory at the next address can be read sequentially by continuing to provide clock pulses to the slave. The internal Address Pointer automatically increments to the next higher address after each byte of data is shifted out. When the highest address is reached, the address counter rolls over to the first valid address allowing the read cycle to be continued indefinitely. The read operation is terminated by raising the CS pin (Figure 1-1).

FIGURE 3-1: EEREAD SEQUENCE



3.2 Nonvolatile Memory Write Sequence

Prior to any attempt to write data to the nonvolatile memory (EEPROM, Unique ID and STATUS register) in the MCP795XXX, the write enable latch must be set by issuing the `EEWREN` instruction (Figure 3-4). This is done by setting $\overline{CS}$ low and then clocking out the proper instruction into the MCP795XXX. After all eight bits of the instruction are transmitted, $\overline{CS}$ must be driven high to set the write enable latch. If the write operation is initiated immediately after the `EEWREN` instruction without $\overline{CS}$ driven high, data will not be written to the array since the write enable latch was not properly set.

After setting the write enable latch, the user may proceed by driving $\overline{CS}$ low, issuing either an `EEWRITE`, `IDWRITE` or a `SWRITE` instruction, followed by the remainder of the address, and then the data to be written. Up to 8 bytes of data can be sent to the device before a write cycle is necessary. The only restriction is that all of the bytes must reside in the same page. Additionally, a page address begins with `XXXX 0000` and ends with `XXXX X111`. If the internal address counter reaches `XXXX X111` and clock signals continue to be applied to the chip, the address counter will roll back to the first address of the page and overwrite any data that previously existed in those locations.

For the data to be actually written to the array, the $\overline{CS}$ must be brought high after the Least Significant bit (D0) of the nth data byte has been clocked in. If $\overline{CS}$ is driven high at any other time, the write operation will not be completed. Refer to Figure 3-2 and Figure 3-3 for more detailed illustrations on the byte write sequence and the page write sequence, respectively. While the nonvolatile memory write is in progress, the STATUS register may be read to check the status of the WIP, WEL, BP1 and BP0 bits. Attempting to read a memory array location will not be possible during a write cycle. Polling the WIP bit in the STATUS register is recommended in order to determine if a write cycle is in progress. When the nonvolatile memory write cycle is completed, the write enable latch is reset.

FIGURE 3-2: BYTE EEWRITE SEQUENCE

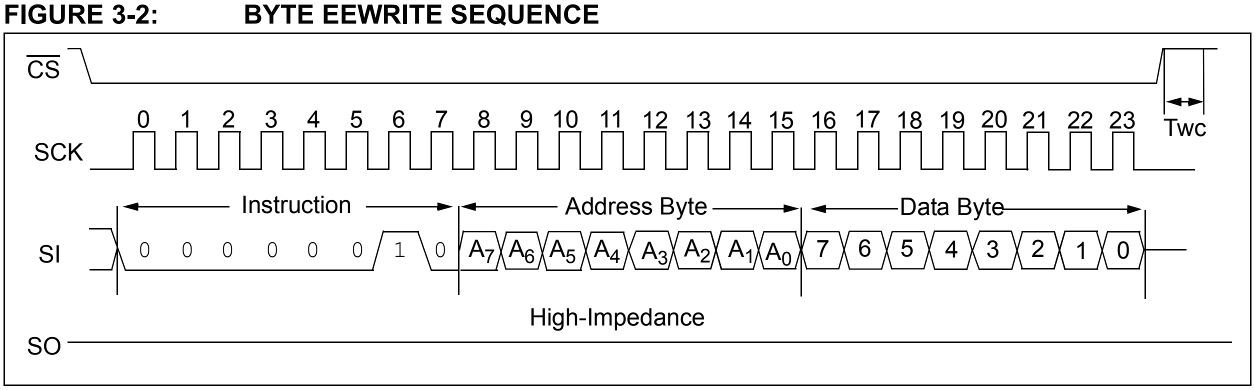
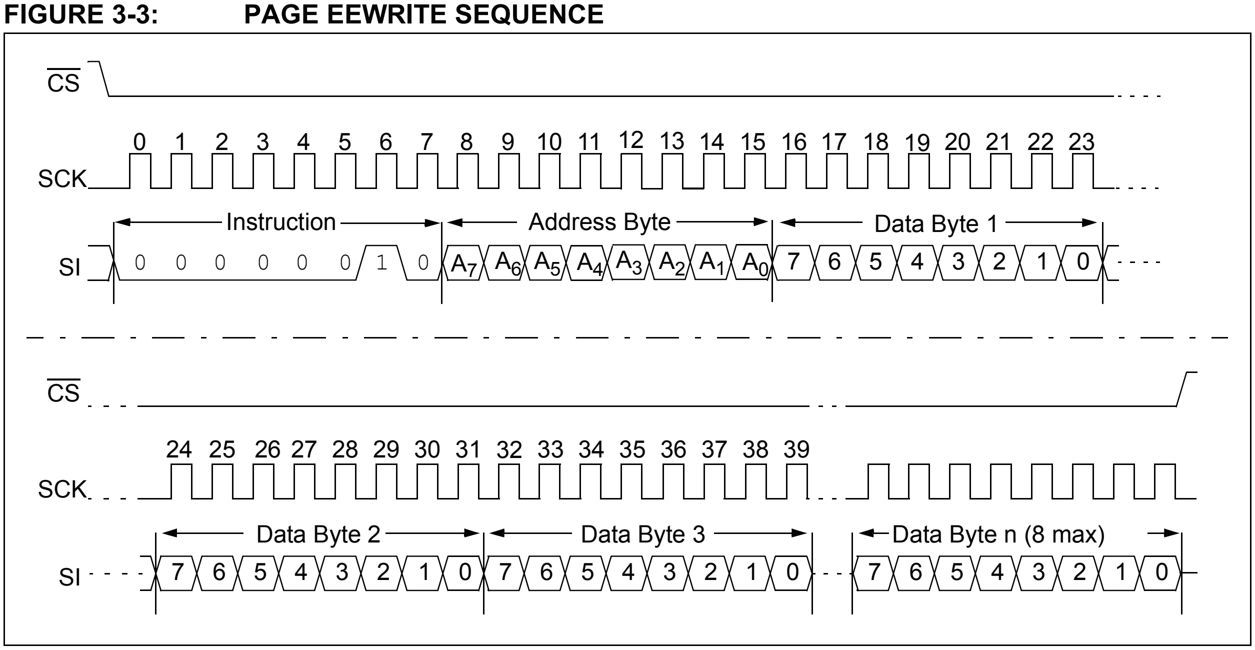


FIGURE 3-3: PAGE EEWRITE SEQUENCE



3.3 Write Enable (EEWREN) and Write Disable (EEWRDI)

The MCP795XXX contains a write enable latch.

This latch must be set before any EEWRITE, SRWRITE and IDWRITE operation will be completed internally. The `EEWREN` instruction will set the latch, and the `EEWRDI` will reset the latch.

The following is a list of conditions under which the write enable latch will be reset:

- Power-up
- `EEWRDI` instruction successfully executed
- `SRWRITE` instruction successfully executed
- `EEWRITE` instruction successfully executed
- `IDWRITE` instruction successfully executed

FIGURE 3-4: WRITE ENABLE SEQUENCE (`EEWREN`)

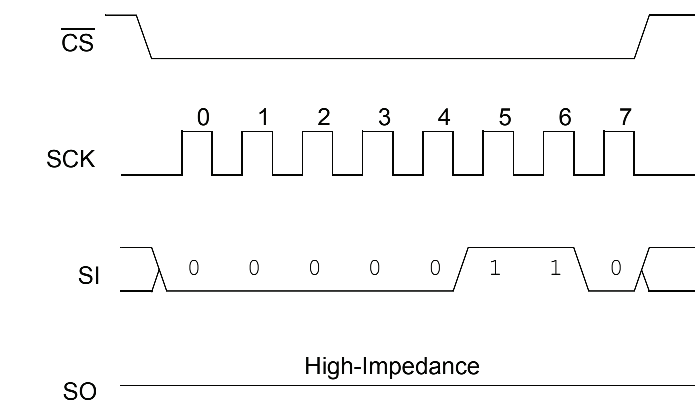
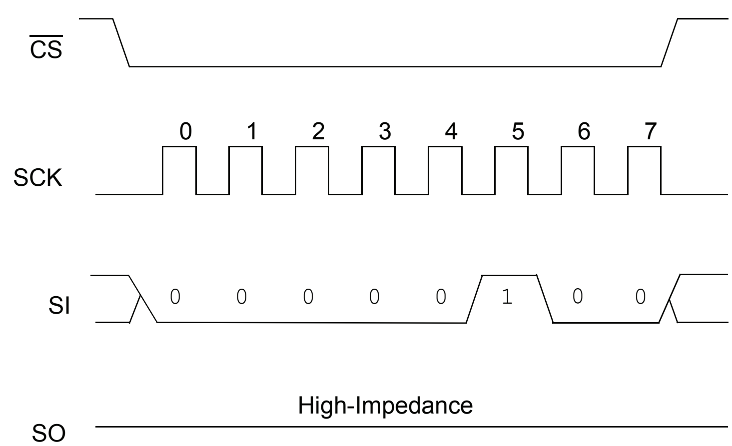


FIGURE 3-5: WRITE DISABLE SEQUENCE (`EEWRDI`)



4.0 RTCC FUNCTIONALITY

4.0.1 RTCC REGISTER MAP

The RTCC register space runs from 0x00 through to 0x1F. Any read or write that is started within the RTCC register address space will wrap to the beginning of the RTCC registers.

All of the RTCC registers are backed up from the VBAT supply when VCC is not available, provided that the VBATEN bit is set. Any unused bits or non implemented addresses read back as '0'. No error checking is provided for any of the RTCC, the user may load any value.

The RTCC register map is shown in Table 4-1.

TABLE 4-1: RTCC REGISTER MAP

Address	BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0	FUNCTION	RANGE
Time and Configuration Registers										
00h	Tenth Seconds				Hundredths of Seconds				Hundredths of seconds	00-99
01h	ST (CT)	10 Seconds			Seconds				Seconds	00-59
02h		10 Minutes			Minutes				Minutes	00-59
03h	CALSGN	12/$\overline{24}$	10 Hour AM/$\overline{PM}$	10 Hour	Hour				Hours	1-12 + AM/$\overline{PM}$ 00 - 23
04h			OSCON	VBAT	VBATEN	Day			Day	1-7
05h			10 Date		Date				Date	01-31
06h			LP	10 Month	Month				Month	01-12
07h	10 Year				Year				Year	00-99
08h	OUT	SQWE	ALM1	ALM0	EXTOSC	RS2	RS1	RS0	Control Reg.	
09h	CALIBRATION								Calibration	
0Ah	WDTEN	WDTIF	WDDEL	WDTPLS	WD3	WD2	WD1	WD0	Watchdog	
0Bh	EVHIF	EVLIF	EVEN1	EVEN0	EVWDT	EVLDB	EVHS1	EVHS0	Event Detect	
Alarm 0 Registers										
0Ch		10 Seconds			Seconds				Seconds	00-59
0Dh		10 Minutes			Minutes				Minutes	00-59
0Eh		12/$\overline{24}$	10 Hour AM/$\overline{PM}$	10 Hours	Hour				Hours	1-12 + AM/$\overline{PM}$ 00-23
0Fh	ALM0PIN	ALM0C2	ALM0C1	ALM0C0	ALM0IF	Day			Day	1-7
10h			10 Date		Date				Date	01-31
11h				10 Month	Month				Month	01-12
Alarm 1 Registers										
12h	Tenth Seconds				Hundredths of seconds				Hundredths of Seconds	00-99
13h		10 Seconds			Seconds				Seconds	00-59
14h		10 Minutes			Minutes				Minutes	00-59
15h		12/$\overline{24}$	10 Hour AM/$\overline{PM}$	10 Hours	Hour				Hours	1-12 + AM/$\overline{PM}$ 00-23
16h	ALM1PIN	ALM1C2	ALM1C1	ALM1C0	ALM1IF	Day			Day	1-7
17h			10 Date		Date				Date	01-31
Power-down Time-stamp Registers										
18h		10 Minutes			Minutes					
19h		12/$\overline{24}$	10 Hour AM/$\overline{PM}$	10 Hours	Hour					
1Ah			10 Date		Date					
1Bh	Day			10 Month	Month					
Power-Up Time-stamp Registers										
1Ch		10 Minutes			Minutes					
1Dh		12/$\overline{24}$	10 Hour AM/$\overline{PM}$	10 Hours	Hour					
1Eh			10 Date		Date					
1Fh	Day			10 Month	Month					

5.0 TIME AND CONFIGURATION REGISTERS

REGISTER 5-1: HUNDREDTHS OF SECONDS 0x00

RW	RW
Tenth Seconds	Hundredths of Seconds
bit 7 bit 4	bit 3 bit 0

Legend: R = Readable Bit W = Writable Bit U = Unimplemented bit, Read as ‘0’

bit 7-4 Tenth Seconds

bit 3-0 Hundredths of Seconds

Note: Contains the BCD Tens and Hundredths of seconds

REGISTER 5-2: SECONDS 0x01

RW	RW	RW
ST (CT)	10 Seconds	Seconds
bit 7	bit 6 bit 4	bit 3 bit 0

Legend: R = Readable Bit W = Writable Bit U = Unimplemented bit, Read as ‘0’

bit 7 ST (CT)
Setting this bit ‘1’ starts the oscillator and clearing this bit ‘0’ stops the on-board oscillator. For the MCP795BXX devices the ST bit is replaced by the CT bit. Setting this bit starts the timekeeping registers counting.

bit 6-4 10 Seconds

bit 3-0 Seconds

Note: Contains the BCD seconds and 10 seconds. The range is 00 to 59.

REGISTER 5-3: MINUTES 0x02

U	RW	RW
	10 Minutes	Minutes
bit 7	bit 6 bit 4	bit 3 bit 0

Legend: R = Readable Bit W = Writable Bit U = Unimplemented bit, Read as ‘0’

bit 7 Unimplemented

bit 6-4 10 Minutes

bit 3-0 Minutes

Note: Contains the BCD minutes and 10 minutes. The range is 00 to 59.

REGISTER 5-4: HOUR 0x03

RW	RW	RW	RW	RW	
CALSGN	12/$\overline{24}$	10 Hour AM/$\overline{PM}$	10 Hour	Hour	
bit 7	bit 6	bit 5	bit 4	bit 3	bit 0

Legend:	R = Readable Bit W = Writable Bit U = Unimplemented bit, Read as ‘0’

bit 7 CALSGN
Bit 7 is the sign bit (CALSGN) for the calibration. Clearing this bit produces a positive calibration, setting this bit produces a negative calibration.

bit 6 12/$\overline{24}$
Clearing this bit to ‘0’ enables 24-hour format, setting this bit ‘1’ enables 12-hour format.

bit 5 10 Hour (AM/$\overline{PM}$ bit for 12-hour time)

bit 4 10 Hour

bit 3-0 Hour

Note: Contains the BCD hour in bits <3:0>. Bits <5:4> contain either the 10-hour in BCD for 24-hour format or the AM/PM indicator and the 10-hour bit for 12-hour format. Bit 5 determines the hour format.

REGISTER 5-5: DAY 0x04

U	U	R	RW	RW	RW	
		OSCON	V_{BAT}	VBATEN	Day	
bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 0

Legend:	R = Readable Bit W = Writable Bit U = Unimplemented bit, Read as ‘0’

bit 7-6 Unimplemented bit, read as ‘0’

bit 5 Bit 5 is the OSCON bit. This is set and cleared by hardware. If this bit is set the oscillator is running, if clear, the oscillator is not running. This bit does not indicate that the oscillator is running at the correct frequency. The bit will wait 32 oscillator cycles before the bit is set.

bit 4 Bit 4 is the V_{BAT} bit. This bit is set by hardware when the V_{CC} fails and the V_{BAT} is used to power the oscillator and the RTCC registers. This bit is cleared by software.

bit 3 Bit 3 is the VBATEN bit. If this bit is set the internal circuitry is connected to the V_{BAT} pin. If this bit is ‘0’ then the V_{BAT} pin is disconnected and the only current drain on the external battery is the V_{BAT} pin leakage.

bit 2-0 Day

Note: Contains the BCD day. The range is 1-7. Also, additional bits are used for configuration and Status.

REGISTER 5-6: DATE 0x05

U	U	RW		RW	
		10 Date		Date	
bit 7	bit 6	bit 5	bit 4	bit 3	bit 0

Legend: R = Readable Bit W = Writable Bit U = Unimplemented bit, Read as ‘0’

bit 7-6 Unimplemented bit, read as ‘0’
bit 5-4 10 Date
bit 3-0 Date
Note: Contains the BCD Date and 10 Date. The range is 01-31.

REGISTER 5-7: MONTH 0x06

U	U	R	RW	RW	
		LP	10 Month	Month	
bit 7	bit 6	bit 5	bit 4	bit 3	bit 0

Legend: R = Readable Bit W = Writable Bit U = Unimplemented bit, Read as ‘0’

bit 7-6 Unimplemented bit, read as ‘0’
bit 5 Bit 5 is the Leap Year bit, this is set during a leap year and is read-only.
bit 4 10 Month
bit 3-0 Month
Note: Contains the BCD month. Bit 4 contains the 10 month.

REGISTER 5-8: YEAR 0x07

RW		RW	
10 Year		Year	
bit 7	bit 4	bit 3	bit 0

Legend: R = Readable Bit W = Writable Bit U = Unimplemented bit, Read as ‘0’

bit 7-4 10 Year
bit 3-0 Year
Note: Contains the BCD Year and 10 Year. The Range is 00-99.

REGISTER 5-9: CONTROL REG 0x08

RW	RW	RW	RW	RW	RW	RW	RW
OUT	SQWE	ALM1	ALM0	EXTOSC	RS2	RS1	RS0
bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0

Legend:	R = Readable Bit W = Writable Bit U = Unimplemented bit, Read as ‘0’

bit 7 Bit 7 is the OUT bit, this sets the logic level on the CLKOUT when not using this as a square wave output.

bit 6 Bit 6 is the SQWE bit, setting this bit enables the divided output from the crystal oscillator.

bit 5:4 ALM1 Bits <5:4> determine which alarms are active.
- `00` – No Alarms are active
- `01` – Alarm 0 is active
- `10` – Alarm 1 is active
- `11` – Both Alarms are active

bit 3 Bit 3 is the EXTOSC enable bit. Setting this bit will allow an external 32.768 kHz signal to drive the RTCC registers, eliminating the need for an external crystal.

bit 2:0 RS2 Bits <2:0> set the internal divider for the 32.768 kHz oscillator to be driven to the CLKOUT. The following frequencies are available. The output is responsive to the Calibration register.
- `000` – 1 Hz
- `001` – 4.096 kHz
- `010` – 8.192 kHz
- `011` – 32.768 kHz
- `1XX` enables the Cal Output function. Cal output appears on CLKOUT if SQWE is set (1 Hz nominal).

Note: When RS2 is set to enable the Cal Output function, the RTCC counters will continue to increment.

REGISTER 5-10: CALIBRATION 0x09

RW	
CALIBRATION	
bit 7	bit 0

Legend:	R = Readable Bit W = Writable Bit U = Unimplemented bit, Read as ‘0’

bit 7-0 Calibration Value

Note: This is an 8-bit register that is used to add or subtract clocks from the RTCC counter every minute. The CALSGN (0x03:7) is the sign bit and indicates if the count should be added or subtracted. The 8 bits in the Calibration register, with each bit adding or subtracting two clocks, gives the user the ability to add or subtract up to 510 clocks per minute.

REGISTER 5-11: WATCHDOG 0x0A

RW	RW	RW	RW	RW	RW	RW	RW
WDTEN	WDTIF	WDDEL	WDTPLS	WD3	WD2	WD1	WD0
bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0

Legend: R = Readable Bit W = Writable Bit U = Unimplemented bit, Read as ‘0’

bit 7 Bit 7 is a read/write bit that is set by the user and can be cleared by the user of the hardware. This bit is set to enable the WDT function and cleared to disable the function. This bit is cleared by the hardware when the VCC supply is not present, it is not set again when VCC is present.

bit 6 Bit 6 is a read/write bit that is set in hardware when the WDT times out and the WD pin is asserted. This bit must be cleared in software to restart the WDT.

bit 5 Bit 5 is a read/write bit and is set to enable a 64-second delay before the WDT starts to count. If this bit is set and the WDTIF bit is cleared then there will be a 64 second delay before the WDT starts to count. This bit should be set before the WDTEN bit is set.

bit 4 Bit 4 is a read/write bit that is used to select the pulse width on the WD pin when the WDT times out.
- 0 – 122 us Pulse
- 1 – 125 ms Pulse

bit 3:0 Bits <3:0> are read/write bits that are used to set the WDT time-out period as below (all times are based off the uncalibrated crystal reference). Bit 3 should be cleared and is reserved for future use:
- 000 – 977 us
- 001 – 15.6 ms
- 010 – 62.5 ms
- 011 – 125 ms
- 100 – 1s
- 101 – 16s
- 110 – 32s
- 111 – 64s

Note: Please see **Section 9.1.3, Watchdog Timer** for more information.

REGISTER 5-12: EVENT DETECT 0x0B

RW	RW	RW	RW	RW	RW	RW	RW
EVHIF	EVLIF	EVEN1	EVEN0	EVWDT	EVLDB	EVHS1	EVHS0
bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0

Legend:	R = Readable Bit W = Writable Bit U = Unimplemented bit, Read as ‘0’

bit 7 When the configured number of high speed events has occurred the $\overline{\text{IRQ}}$ pin is asserted and the EVHIF bit is set in hardware. The clear the $\overline{\text{IRQ}}$ pin and reset the EVHIF bit must be cleared in software.

bit 6 When an event occurs on the low-speed pin this $\overline{\text{IRQ}}$ pin is asserted and the EVLIF bit is set. This bit must be cleared by software to reset the module and clear the $\overline{\text{IRQ}}$ pin.

bit 5:4 <1:0> These two bits determine what combination of the high and low-speed modules are enabled.
- `00` – Both modules are Off
- `01` – Low-speed module enabled, high speed disabled
- `10` – Low-speed module disabled, high speed enabled
- `11` – Both modules are enabled

bit 3 Setting this bit overrides any setting for the High-Speed Event Detection and allows the EVHS pin to clear the Watchdog Timer. This is edge triggered. Either and H-L or L-H transition will clear the WDT.

bit 2 This is the Low-Speed Event Debounce setting. Depending on the state of this bit the low-speed pin will have to remain at the same state for the following periods to be considered valid.
- `0` – 31.25 ms
- `1` – 500 ms

bit 1:0 EVHS <1:0> These bits determine how many high-speed events must occur before the EVHIF bit is set. All of these events must occur within 250 ms (based on the uncalibrated 32.768 kHz clock).
- `00` – 1st Event
- `01` – 4th Event
- `10` – 16th Event
- `11` – 32nd Event

Note: Please see **Section 9.1.4, Event Detection** for more information.

6.0 ALARM 0 REGISTERS

REGISTER 6-1: SECONDS 0x0C

RW	RW	RW
	10 Seconds	Seconds
bit 7	bit 6 bit 4	bit 3 bit 0

Legend: R = Readable Bit W = Writable Bit U = Unimplemented bit, Read as ‘0’

bit 7 Unimplemented
bit 6-4 10 Seconds
bit 3-0 Seconds
Note: This contains the seconds match for the Alarm 0.

REGISTER 6-2: MINUTES 0x0D

RW	RW	RW
	10 Minutes	Minutes
bit 7	bit 6 bit 4	bit 3 bit 0

Legend: R = Readable Bit W = Writable Bit U = Unimplemented bit, Read as ‘0’

bit 7 Unimplemented
bit 6-4 10 Minutes
bit 3-0 Minutes
Note: This contains the minutes match for the Alarm 0.

REGISTER 6-3: HOURS 0x0E

RW	RW			RW
	12/$\overline{24}$	10 Hour AM/$\overline{PM}$	10 Hour	Hour
bit 7	bit 6	bit 5	bit 4	bit 3 bit 0

Legend: R = Readable Bit W = Writable Bit U = Unimplemented bit, Read as ‘0’

bit 7 Unimplemented
bit 6 12/$\overline{24}$ (this is a copy of bit 6 in the Hours register (0x03)
bit 5 10 Hour AM/$\overline{PM}$
bit 4 10 Hour
bit 3-0 Hour

REGISTER 6-4: DAY 0x0F

RW	RW			RW	RW
ALM0PIN	ALM0C2	ALM0C1	ALM0C0	ALM0IF	Day
bit 7	bit6		bit 4	bit 3	bit 2 bit 0

Legend: R = Readable Bit W = Writable Bit U = Unimplemented bit, Read as ‘0’

bit 7 Bit 7 configures the pin that is used for the Alarm 0 output. If this bit is clear the $\overline{IRQ}$ pin is used. If set, the $\overline{WDO}$ pin is used. If the WDT is enabled then a valid Alarm will assert the $\overline{WDO}$ pin for 122 us.

BIT 6:4 Bits <6:4> sets the condition on what the Alarm will trigger. The following options are available:
`000` – Seconds match
`001` – Minutes match
`010` – Hours match (logic takes into account 12/24 operation)
`011` – Day match. Generates interrupt at 12:00:00 AM
`100` – Date match
`101` – Unimplemented, do not use
`110` – Unimplemented, do not use
`111` – Seconds, Minutes, Hour, Day, Date and Month

bit 3 Bit 3 is the ALM0IF bit. This is set by hardware when an alarm condition has be generated. The bit must be cleared in software.

bit 2-0 Day

REGISTER 6-5: DATE 0x10

U	U	RW	RW	RW
		10 Date		Date
bit 7	bit 6	bit 5	bit 4	bit 3 bit 0

Legend: R = Readable Bit W = Writable Bit U = Unimplemented bit, Read as ‘0’

bit 7-6 Unimplemented

bit 5-4 10 Date

bit 3-0 Date

REGISTER 6-6: MONTH 0x11

U	U	U	RW	RW
			10 Month	Month
bit 7	bit 6	bit 5	bit 4	bit 3 bit 0

Legend: R = Readable Bit W = Writable Bit U = Unimplemented bit, Read as ‘0’

bit 7-5	Unimplemented
bit 4	10 Month
bit 3-0	Month
Note:	Month match is only available on Alarm 0.

 Preliminary

7.0 ALARM 1 REGISTERS

REGISTER 7-1: HUNDREDTHS OF SECONDS 0x12

RW		RW	
Tenth Seconds		Hundredths of Seconds	
bit 7	bit 4	bit 3	bit 0

Legend: R = Readable Bit W = Writable Bit U = Unimplemented bit, Read as '0'

bit 7-4 Tenth Seconds

bit 3-0 Hundredths of Seconds

Note: Hundredths and Tenth seconds only available on Alarm 1.

REGISTER 7-2: SECONDS 0x13

U	RW		RW	
	10 Seconds		Seconds	
bit 7	bit 6	bit 4	bit 3	bit 0

Legend: R = Readable Bit W = Writable Bit U = Unimplemented bit, Read as '0'

bit 7 Unimplemented

bit 6-4 10 Seconds

bit 3-0 Seconds

REGISTER 7-3: MINUTES 0x14

U	RW		RW	
	10 Minutes		Minutes	
bit 7	bit 6	bit 4	bit 3	bit 0

Legend: R = Readable Bit W = Writable Bit U = Unimplemented bit, Read as '0'

bit 7 Unimplemented

bit 6-4 10 Minutes

bit 3-0 Minutes

REGISTER 7-4: HOURS 0x15

U	RW	RW	RW	RW
	12/$\overline{24}$	10 Hour AM/$\overline{\text{PM}}$	10 Hour	Hour
bit 7	bit 6	bit 5	bit 4	bit 3 bit 0

Legend: R = Readable Bit W = Writable Bit U = Unimplemented bit, Read as ‘0’

bit 7 Unimplemented

bit 6 12/$\overline{24}$

bit 5 10 Hour AM/$\overline{\text{PM}}$

bit 4 10 Hour

bit 3-0 Hour

REGISTER 7-5: DAY 0x16

RW	RW	RW	RW	RW	RW
ALM1PIN	ALM1C2	ALM1C1	ALM1C0	ALM1IF	Day
bit 7	bit 6	bit 5	bit 4	bit 3	bit 2 bit 0

Legend: R = Readable Bit W = Writable Bit U = Unimplemented bit, Read as ‘0’

bit 7 Bit 7 configures the pin that is used for the Alarm 0 output. If this bit is clear the $\overline{\text{IRQ}}$ pin is used. If set, the $\overline{\text{WDO}}$ pin is used. If the WDT is enabled then a valid Alarm will assert the $\overline{\text{WDO}}$ pin for 122 us.

BIT 6:4 Bits <6:4> sets the condition on what the Alarm will trigger. The following options are available:
`000` – Seconds match
`001` – Minutes match
`010` – Hours match (logic takes into account 12/24 operation)
`011` – Day match, generates interrupt at 12:00:00 am
`100` – Date match
`101` – Hundredths/Tenth of Seconds
`110` – Unimplemented do not use
`111` – Seconds, Minutes, Hour, Day and Date

bit 3 Bit 3 is the ALM1IF bit. This is set by hardware when an alarm condition has be generated. The bit must be cleared in software.

bit 2-0 Day

REGISTER 7-6: DATE 0x17

U	U	RW		RW			
		10 Date		Date			
bit 7	bit 6	bit 5	bit 4	bit 3			bit 0

Legend: R = Readable Bit W = Writable Bit U = Unimplemented bit, Read as ‘0’

bit 7-6	Unimplemented
bit 5-4	10 Date
bit 3-0	Date

8.0 POWER-DOWN TIME-STAMP REGISTERS

Note:	It is strongly recommended that the timesaver function only be used when the oscillator is running. This will ensure accurate functionality.

REGISTER 8-1: MINUTES 0x18

U	RW	RW
	10 Minutes	Minutes
bit 7	bit 6 bit 4	bit 3 bit 0

Legend: R = Readable Bit W = Writable Bit U = Unimplemented bit, Read as '0'

bit 7 Unimplemented
bit 6-4 10 Minutes
bit 3-0 Minutes

REGISTER 8-2: HOUR 0x19

U	RW	RW	RW	RW
	12/$\overline{24}$	10 Hour AM/$\overline{PM}$	10 Hours	Hour
bit 7	bit 6	bit 5	bit 4	bit 3 bit 0

Legend: R = Readable Bit W = Writable Bit U = Unimplemented bit, Read as '0'

bit 7 Unimplemented
bit 6 12/$\overline{24}$ (this is a copy of the status of the bit in register 0x03:6 at the time of the event)
bit 5 10 Hour AM/$\overline{PM}$
bit 4 10 Hour
bit 3-0 Hour

REGISTER 8-3: DATE 0x1A

U	U	RW	RW	RW
		10 Date		Date
bit 7	bit 6	bit 5	bit 4	bit 3 bit 0

Legend: R = Readable Bit W = Writable Bit U = Unimplemented bit, Read as '0'

bit 7-6 Unimplemented
bit 5-4 10 Date
bit 3-0 Date

REGISTER 8-4: MONTH 0x1B

RW	RW	RW	RW	RW
Day			10 Month	Month
bit 7	bit 6	bit 5	bit 4	bit 3 bit 0

Legend: R = Readable Bit W = Writable Bit U = Unimplemented bit, Read as ‘0’

bit 7-5 Day
bit 4 10 Month
bit 3-0 Month

9.0 POWER-UP TIME REGISTERS

Note:	It is strongly recommended that the timesaver function only be used when the oscillator is running. This will ensure accurate functionality.

REGISTER 9-1: MINUTES 0x1C

U	RW		RW	
	10 Minutes		Minutes	
bit 7	bit 6	bit 4	bit 3	bit 0

Legend: R = Readable Bit W = Writable Bit U = Unimplemented bit, Read as ‘0’

bit 7 Unimplemented
bit 6-4 10 Minutes
bit 3-0 Minutes

REGISTER 9-2: HOUR 0x1D

U	RW	RW	RW	RW	
	$12/\overline{24}$	10 Hour AM/$\overline{PM}$	10 Hours	Hour	
bit 7	bit 6	bit 5	bit 4	bit 3	bit 0

Legend: R = Readable Bit W = Writable Bit U = Unimplemented bit, Read as ‘0’

bit 7 Unimplemented
bit 6 $12/\overline{24}$ (this is a copy of the status of the bit in register 0x03:6 at the time of the event)
bit 5 10 Hour AM/$\overline{PM}$
bit 4 10 Hour
bit 3-0 Hour

REGISTER 9-3: DATE 0x1E

U	U	RW	RW	RW	
		10 Date		Date	
bit 7	bit 6	bit 5	bit 4	bit 3	bit 0

Legend: R = Readable Bit W = Writable Bit U = Unimplemented bit, Read as ‘0’

bit 7-6 Unimplemented
bit 5-4 10 Date
bit 3-0 Date

REGISTER 9-4: MONTH 0x1F

RW	RW	RW	RW	RW	
Day			10 Month	Month	
bit 7	bit 6	bit 5	bit 4	bit 3	bit 0

Legend: R = Readable Bit W = Writable Bit U = Unimplemented bit, Read as ‘0’

bit 7-5 Day
bit 4 10 Month
bit 3-0 Month

9.1 Features

9.1.1 CALIBRATION

The Calibration register (0x09h) allows a number of RTCC counts to be added or subtracted (Cal Sign bit located at 0x03:7) each minute. This allows for calibration to reduce the PPM error due to oscillator shift. This register is volatile.

The CALSIGN determines if calibration is positive or negative.

A value of 0x00 in the Calibration register will result in no calibration.

The calibration is linear, with one bit representing two RTC clocks.

The MCP795XXX utilizes digital calibration to correct for the inaccuracies of the input clock source (either external or crystal). Calibration is enabled by setting the value of the Calibration register at address 08H. Calibration is achieved by adding or subtracting a number of input clock cycles per minute in order to achieve ppm level adjustments in the internal timing function of the MCP795XXX.

The CALSGN bit is the sign bit, with a ‘1’ indicating subtraction and a ‘0’ indicating addition. The eight bits in the calibration register indicate the number of input clock cycles (multiplied by two) that are subtracted or added per minute to the internal timing function.

The internal timing function can be monitored using the CLKOUT output pin by setting bit 6 (SQWE) and bits <2:0> (RS2, RS1, RS0) of the Control register at address 07H. Note that the CLKOUT output waveform is disabled when the MCP795XXX is running in VBAT mode. With the SQWE bit set to ‘1’, there are two methods that can be used to observe the internal timing function of the MCP795XXX:

A. RS2 bit set to ‘0’

With the RS2 bit set to ‘0’, the RS1 and RS0 bits enable the following internal timing signals to be output on the CLKOUT pin:

RS2	RS1	RS0	Output Signal
0	0	0	1 Hz
0	0	1	4.096 kHz
0	1	0	8.192 kHz
0	1	1	32.768 kHz

The frequencies listed in the table presume an input clock source of exactly 32.768 kHz. In terms of the equivalent number of input clock cycles, the table becomes:

RS2	RS1	RS0	Output Signal
0	0	0	32768
0	0	1	8
0	1	0	4
0	1	1	1

With regards to the calibration function, the Calibration register setting has no impact upon the CLKOUT output clock signal when bits RS1 and RS0 are set to ‘11’. The setting of the calibration register to a non-zero value enables the calibration function which can be observed on the CLKOUT output pin. The calibration function can be expressed in terms of the number of input clock cycles added/subtracted from the internal timing function.

With bits RS1 and RS0 set to ‘00’, the calibration function can be expressed as:

$$T_{output} = (32768 +/- (2 * CALREG))\ T_{input}$$

where:

T_{output} = clock period of CLKOUT output signal

T_{input} = clock period of input signal

CALREG = decimal value of calibration register setting and the sign is determined by the CALSGN bit.

Since the calibration is done once per minute (i.e. when the internal minute counter is incremented), only one cycle in sixty of the CLKOUT output waveform is affected by the calibration setting. Also note that the duty cycle of the CLKOUT output waveform will not necessarily be at 50% when the calibration setting is applied.

With bits RS1 and RS0 set to ‘01’ or ‘10’, the calibration function can not be expressed in terms of the input clock period. In the case where the MSB of the Calibration register is set to ‘0’, the waveform appearing at the CLKOUT output pin will be “delayed”, once per minute, by twice the number of input clock cycles defined in the Calibration register. The CLKOUT waveform will appear as shown in Figure 9-1.

In the case where the MSB of the Calibration register is set to '1', the CLKOUT output waveforms that appear when bits RS1 and RS0 are set to '01' or '10' are not as responsive to the setting of the Calibration register. For example, when outputting the 4.096 kHz waveform (RS1, RS0 set to '01'), the output waveform is generated using only eight input clock cycles. Consequently, attempting to subtract more than eight input clock cycles from this output does not have a meaningful affect on the resulting waveform. Any affect on the output will appear as a modification in both the frequency and duty cycle of the waveform appearing on the CLKOUT output pin.

B.RS2 bit set to '1'

With the RS2 bit set to '1', the following internal timing signal is output on the CLKOUT pin:

RS2	RS1	RS0	Output Signal
1	x	x	1.0 Hz

The frequency listed in the table presumes an input clock source of exactly 32.768 kHz. In terms of the equivalent number of input clock cycles, the table becomes:

RS2	RS1	RS0	Output Signal
1	x	x	32768

Unlike the method previously described, the calibration setting is continuously applied and affects every cycle of the output waveform. This results in the modulation of the frequency of the output waveform based upon the setting of the Calibration register.

Using this setting, the calibration function can be expressed as:

$$T_{output} = (32768 \text{ +/- } (2 * CALREG))\, T_{input}$$

where:

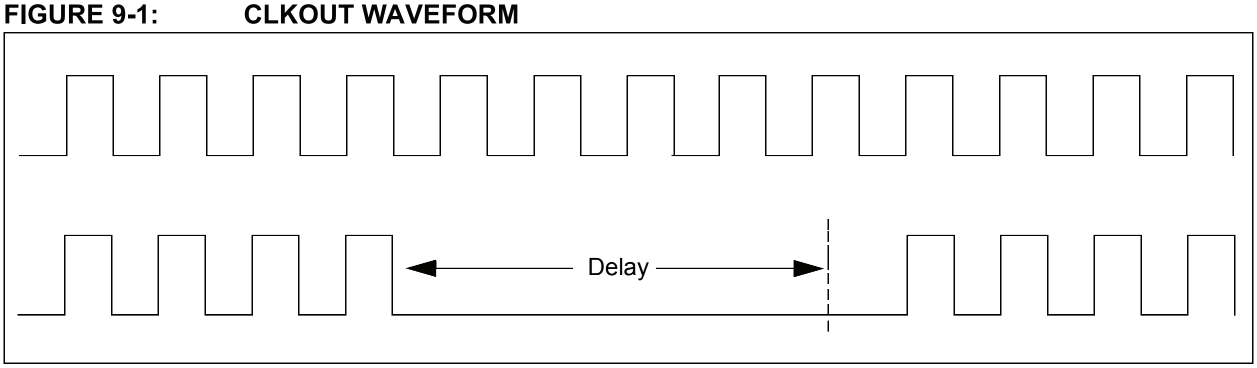
T_{output} = clock period of CLKOUT output signal

T_{input} = clock period of input signal

CALREG = decimal value of calibration register setting and the sign is determined by the CALSGN bit.

Since the calibration is done every cycle, the frequency of the output CLKOUT waveform is constant.

FIGURE 9-1: CLKOUT WAVEFORM



9.1.2 CLOCKOUT FUNCTION

The MCP795W20 features a push-pull pin CLKOUT that can supply a digital signal based on a division of the main 32.768 kHz clock. If this function is not used the pin may be directly controlled using the OUT bit in the Control register (0x08). In V_{BAT} mode, CLKOUT is logic low. In V_{DD} POR condition, the CLKOUT is tri-stated. For the MCP795BXX devices, this pin functions as a Power-up Boot clock. A 32.768 kHz clock is enabled upon application of V_{CC}.

9.1.3 WATCHDOG TIMER

The on-board Watchdog Timer is configured by loading the register at address 0x0A. The WDT is not available when the MCP795XXX is operating from the V_{BAT} supply. When in this condition, the WDT is disabled by the hardware and must be re-enabled when V_{CC} is restored. The output of the WDT is based on the uncalibrated 32.768 kHz oscillator.

Description of WDT Bits:

- Bit 7 is a read/write bit that is set and cleared by software. This bit is set to enable the WDT function and cleared to disable the function. A V_{CC} power fail will cause this bit to be cleared and not re-enabled when V_{CC} is restored.
- Bit 6 is a read/write bit that is set in hardware when the WDT times out and the $\overline{\text{WDO}}$ pin is asserted. This bit must be cleared in software to restart the WDT.
- Bit 5 is a read/write bit and is set to enable a 64-second delay before the WDT starts to count. If this bit is set and the WDTIF bit is cleared then there will be a 64-second delay before the WDT starts to count. This bit should be set before the WDTEN bit is set.
- Bit 4 is a read/write bit that is used to select the pulse width on the $\overline{\text{WDO}}$ pin when the WDT times out.
  - `0` – 122 us Pulse
  - `1` – 125 ms Pulse
- Bits <3:0> are read/write bits that are used to set the WDT time-out period as below (all times are based off the uncalibrated crystal reference). Bit 3 should be cleared and is reserved for future use:
  - `000` – 977 us
  - `001`– 15.6 ms
  - `010` – 62.5 ms
  - `011` – 125 ms
  - `100` – 1s
  - `101` – 16s
  - `110` – 32s
  - `111` – 64s

To reset the WDT the `CLRWDT` instruction must be issued over the SPI interface, as shown in Figure 9-7. If the WDT is not cleared with the CLRWDT command before time-out then the $\overline{\text{WDO}}$ pin will assert and the WDTIF bit will be set. The WDTIF bit must be cleared by software to restart the WDT.

9.1.4 EVENT DETECTION

The on-chip event detection consists of two separate detection circuits.

The high-speed circuit is designed to operate with a digital signal from the output of an external signal conditioning circuit. The input is edge triggered, and will generate an interrupt when the correct number of events has occurred.

The low-speed circuit is designed to operate directly with mechanical switches and support built-in switch debounce.

Registers associated with the event detection module:

- EVHIF – When the configured number of high speed events has occurred the $\overline{\text{IRQ}}$ pin is asserted and the EVHIF bit is set. This bit must be cleared by software to reset the module and clear the $\overline{\text{IRQ}}$ pin.
- EVLIF – When an event occurs on the low-speed pin this $\overline{\text{IRQ}}$ pin is asserted and the EVLIF bit is set. This bit must be cleared by software to reset the module and clear the $\overline{\text{IRQ}}$ pin.
- EVEN<1:0> – These two bits determine what combination of the high and low-speed modules are enabled.
  - `00` – Both modules are off
  - `01` – Only low-speed module enabled
  - `10` – Only high-speed module disabled
  - `11` – Both modules are enabled
- EVWDT – setting this bit overrides any setting for the High-Speed Event Detection and allows the EVHS pin to clear the Watchdog Timer. This is edge triggered. Either H-L or L-H transition will clear the WDT.
- EVLDB – This is the low-speed event debounce setting. Depending on the state of this bit the low-speed pin will have to remain at the same state for the following periods to be considered valid.
  - `0` – 31.25 ms
  - `1` – 500 ms

The debounce will only operate if the clock is running and these timings are based on the uncalibrated 32.768 kHz clock.

- EVHS<1:0> – These bits determine how many high-speed events must occur before the EVHIF bit is set. All of these events must occur within 250 ms.
  - `00` – 1st Event
  - `01` – 4th Event
  - `10` – 16th Event
  - `11` – 32nd Event

9.1.5 VBAT SWITCHOVER

If the V_{BAT} feature is not used, the V_{BAT} pin should be connected to GND. A low value series resistor and Schottky diode are recommended between the external battery and the V_{BAT} pin to reduce inrush current and also to prevent any leakage current reaching the external V_{BAT} source.

The V_{TRIP} point is defined as 1.5V typical. When V_{DD} falls below 1.5V the system will continue to operate the RTCC and SRAM using the V_{BAT} supply. There is ~50mV hyst in the trip point changeover. The following conditions apply:

TABLE 9-1: VBAT CHANGOVER CONDITIONS

Supply Condition	Read/Write Access	Powered By
$V_{CC} < V_{TRIP}$, $V_{CC} < V_{BAT}$	No	V_{BAT}
$V_{CC} > V_{TRIP}$, $V_{CC} < V_{BAT}$	Yes	V_{CC}
$V_{CC} > V_{TRIP}$, $V_{CC} > V_{BAT}$	Yes	V_{CC}

For more information on V_{BAT} conditions see the RTCC Best Practices Application Note, AN1365 (DS01365).

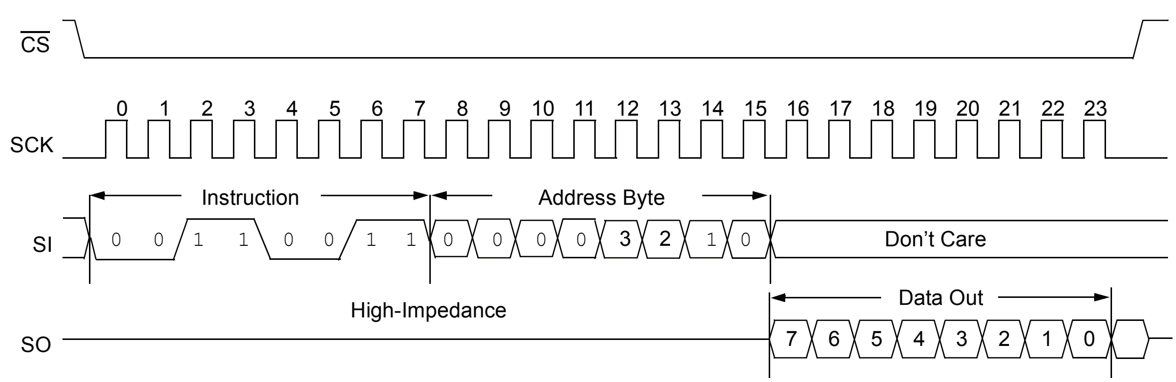
9.1.6 UNIQUE ID LOCATIONS

When the unique ID locations are preprogrammed from the factory with either an EUI-48 or EUI-64, the EUI code is programmed into location 0x00-0x07. Locations 0x08-0x0F are blank (0x0F).

> **Note:** For EUI-64, the data is located in address 0x00-0x07. For EUI-48 locations, 0x02-0x07 contain the data. 0x00/01 contain 0xFF.

To read the unique ID location the IDREAD command is given with the starting address. Valid addresses are 0x00 through 0x0F. All 16 bytes can be read out in a single command by clocking the device. Trying to access locations past 0x0F will result in the address wrapping within these 16 bytes.

FIGURE 9-2: IDREAD COMMAND SEQUENCE

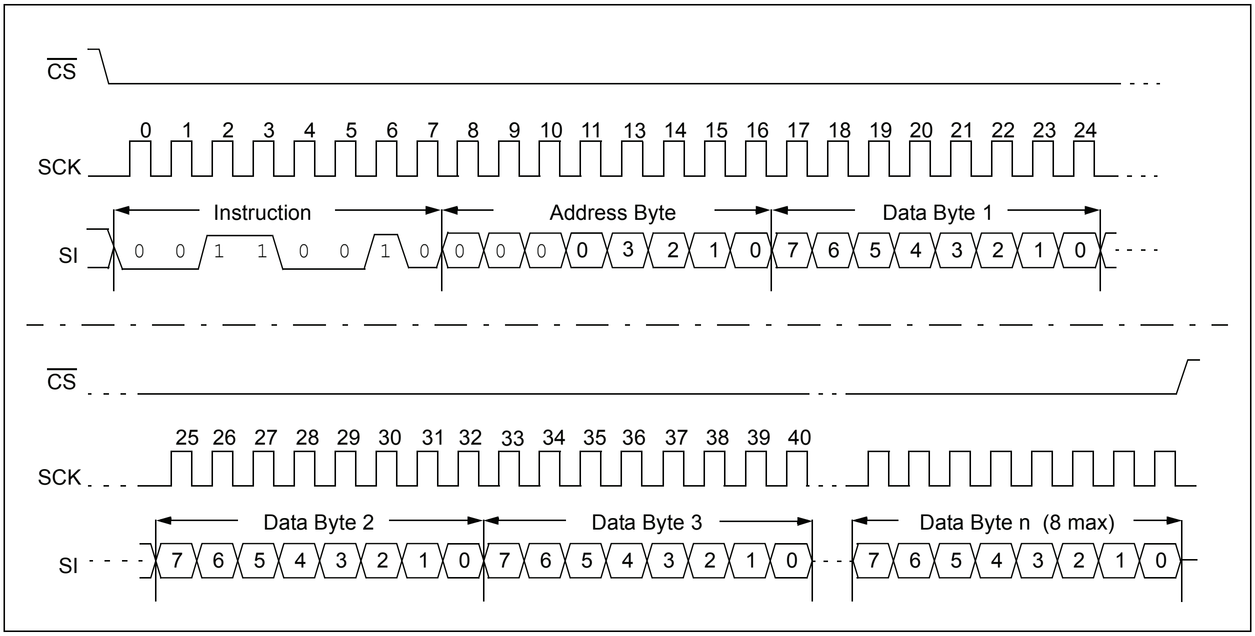


Address range is 0x00-0x0F, address counter will wrap within this range.

To write to the unique ID locations, the IDWRITE command is used. The device must be write enabled and the correct unlock sequence must have been performed. See **Section 10.1.4, Write to the Unlock Register** for more details.

The ID locations can be written to using the IDWRITE command. The valid address is between 0x00 and 0x0F. The entire 16 bytes must be written in two groups of 8 bytes. A maximum of 8 bytes can be written at once.

FIGURE 9-3: IDWRITE COMMAND SEQUENCE



 Preliminary

9.1.7 POWER-FAIL TIME-STAMP

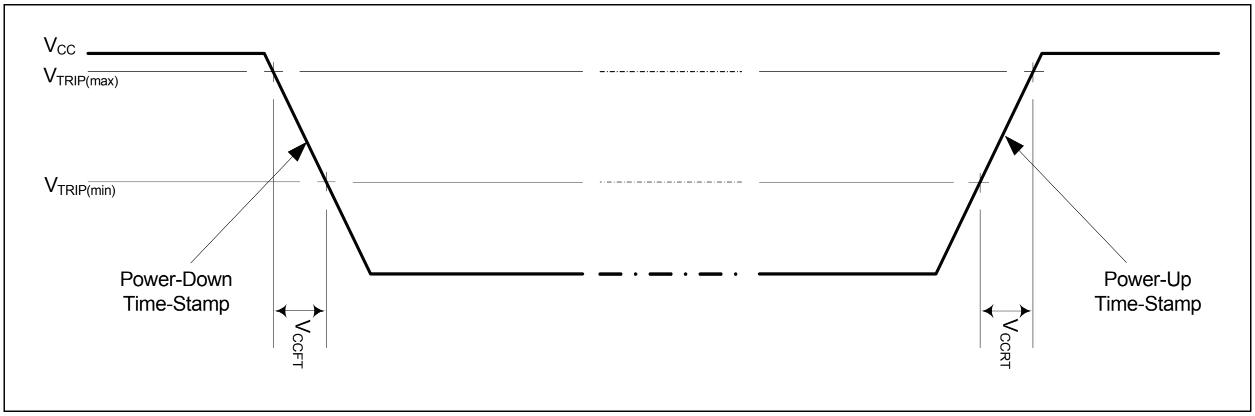
The MCP795XXX family of RTCC devices feature a power-fail time-stamp feature. This feature will save the time at which VCC crosses the VTRIP voltage and is shown in Figure 9-4. To use this feature, a VBAT supply must be present and the oscillator must also be running. There are two separate sets of registers that are used to record this information:

- The first set located at 0x18h through 0x1Bh are loaded at the time when VCC falls below VTRIP and the RTCC operates on the VBAT. The VBAT (register 0x03h bit 4) bit is also set at this time.
- The second set of registers, located at 0x1Ch through 0x1Fh, are loaded at the time when VCC is restored and the RTCC switches to VCC.

The power-fail time-stamp registers are cleared when the VBAT bit is cleared in software.

Note:	It is strongly recommended that the time-saver function only be used when the oscillator is running. This will ensure accurate functionality

FIGURE 9-4: POWER-FAIL GRAPH



9.1.8 READ STATUS REGISTER (SRREAD)

The Read Status Register (`SRREAD`) instruction provides access to the STATUS register. The STATUS register may be read at any time, even during a write cycle. The STATUS register is formatted as follows:

7	6	5	4	3	2	1	0
—	—	—	—	R/W	R/W	R	R
X	X	X	X	BP1	BP0	WEL	WIP

.

Note:	Once a Write Status Register is initiated and a Read Status Register is attempted the new values for the nonvolatile bits will be read regardless of whether the values have been actually programmed into the device. (i.e., The values are moved to the latches prior to the write operation).

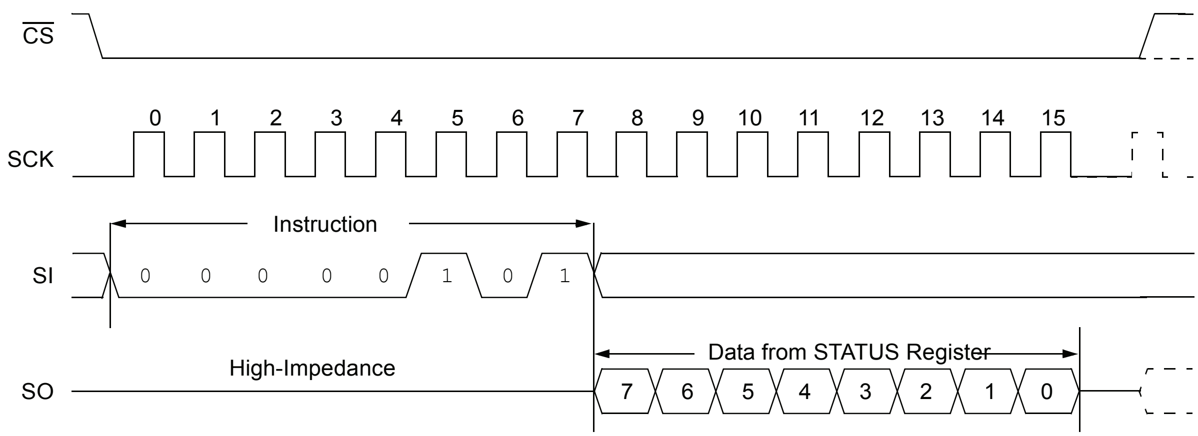
The **Write-In-Process (WIP)** bit indicates whether the MCP795XXX is busy with a nonvolatile memory write operation. When set to a ‘`1`’, a write is in progress, when set to a ‘`0`’, no write is in progress. This bit is read-only.

The **Write Enable Latch (WEL)** bit indicates the status of the write enable latch. When set to a ‘`1`’, the latch allows writes to the nonvolatile memory, when set to a ‘`0`’, the latch prohibits writes to the nonvolatile memory. The state of this bit can always be updated via the WREN or WRDI commands, regardless of the state of write protection on the STATUS register. This bit is read-only.

The **Block Protection (BP0 and BP1)** bits indicate which blocks are currently write-protected. These bits are set by the user issuing the `WRSR` instruction. These bits are nonvolatile.

See Figure 9-5 for the RDSR timing sequence.

FIGURE 9-5: READ STATUS REGISTER TIMING SEQUENCE



* Data should be able to continuously be read from the STATUS register without toggling $\overline{CS}$, for updating of the WIP and WEL bits.

9.1.9 WRITE STATUS REGISTER (SRWRITE)

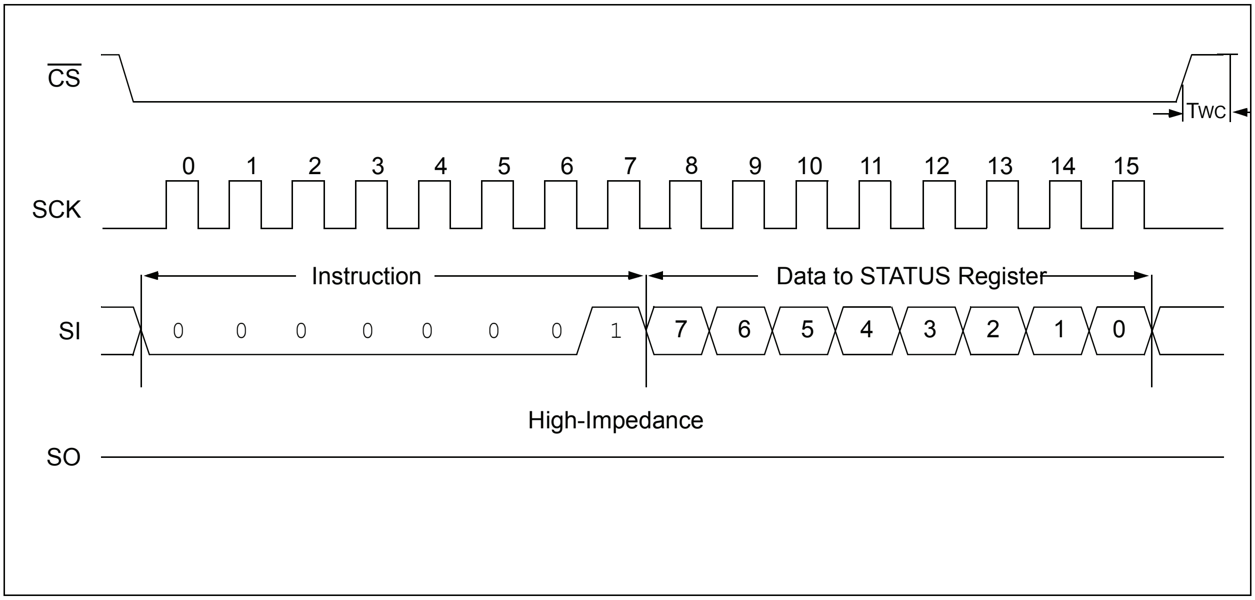
The Write Status Register (`SRWRITE`) instruction allows the user to select one of four levels of protection for the array by writing to the appropriate bits in the status register. The array is divided up into four segments. The user has the ability to write protect none, one, two, or all four of the segments of the array. The partitioning is controlled as shown in Table 9-2.

See Figure 9-6 for the SRWRITE timing sequence.

TABLE 9-2: ARRAY PROTECTION

BP1	BP0	Array Addresses Write-Protected (2 kbit shown)
0	0	none
0	1	upper 1/4 (C0h-FFh)
1	0	upper 1/2 (80h-FFh)
1	1	all (00h-FFh)

FIGURE 9-6: WRITE STATUS REGISTER TIMING SEQUENCE



9.1.10 DATA PROTECTION

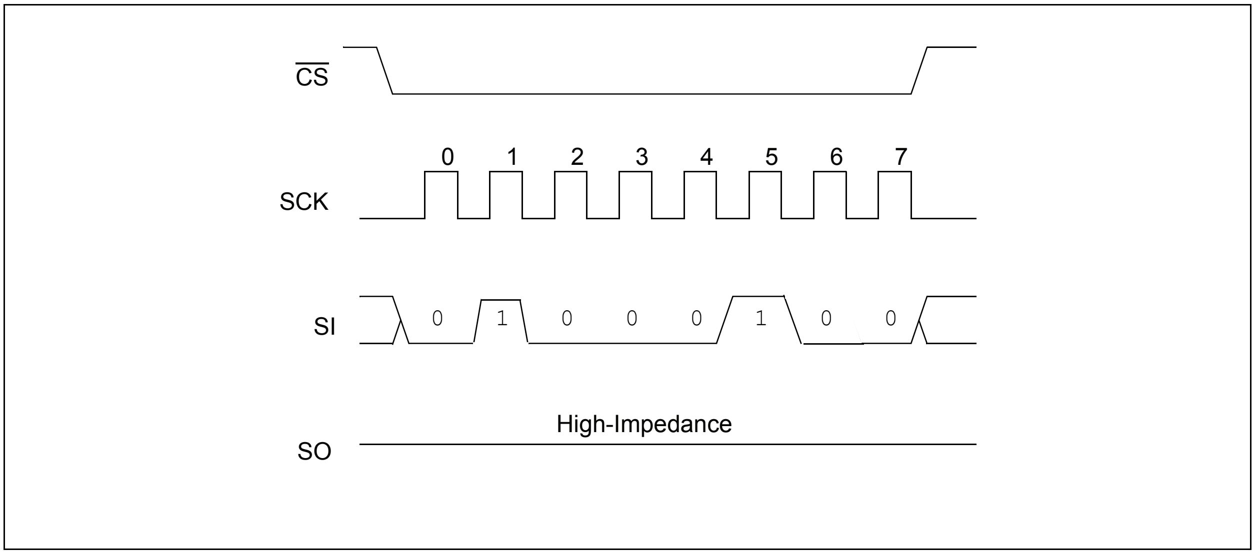
The following protection has been implemented to prevent inadvertent writes to the array:

- The write enable latch is reset on power-up
- A Write Enable instruction must be issued to set the write enable latch
- After a byte write, page write, unique ID write, or STATUS register write, the write enable latch is reset
- $\overline{CS}$ must be set high after the proper number of clock cycles to start an internal write cycle
- Access to the array during an internal EEPROM write cycle is ignored and programming is continued
- Block protect bits are ignored for UID writes

9.1.11 CLEAR WATCHDOG INSTRUCTION

The Clear Watchdog command resets the internal Watchdog Timer.

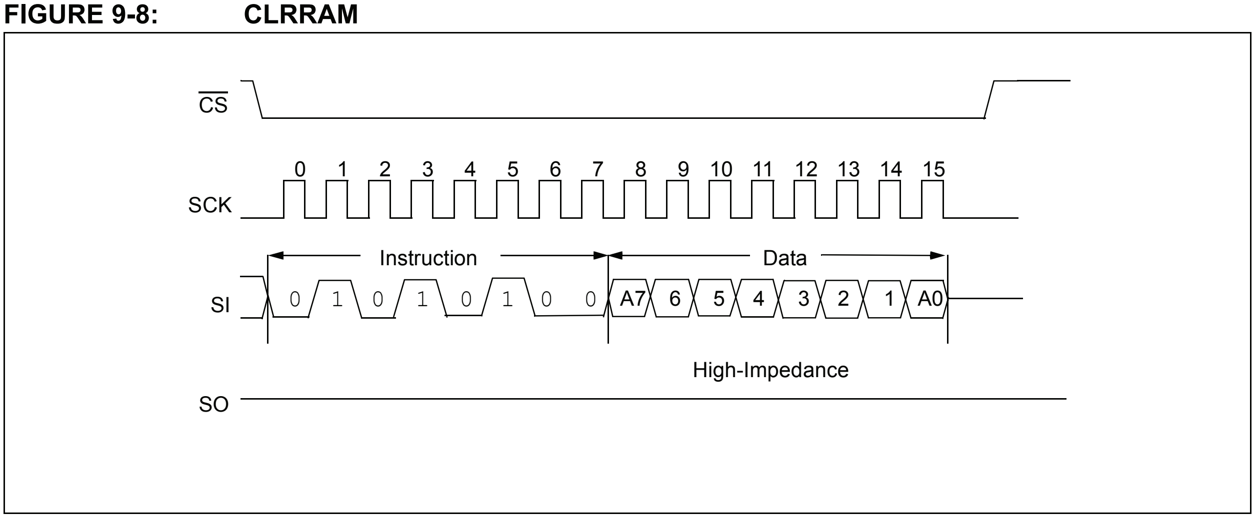
FIGURE 9-7: CLRWDT



9.1.12 CLEAR RAM INSTRUCTION

The Clear Ram instruction is a 2-byte command that will reset the internal SRAM to the known value. Using this command, all locations in the SRAM are set to 00h and the data value contained in the second byte of the command is ignored.

FIGURE 9-8: CLRRAM



9.2 Crystal Specification and Selection

The MCP795XXX has been designed to operate with a standard 32.768 kHz tuning fork crystal. The on-board oscillator has been characterized to operate with a crystal of maximum ESR of 70K Ohms.

Crystals with a comparable specification are also suitable for use with the MCP795XXX.

The table below is given as design guidance and a starting point for crystal and capacitor selection.

Manufacturer	Part Number	Crystal Capacitance	CX1 Value	CX2 Value
Micro Crystal	CM7V-T1A	7pF	10pF	12pF
Citizen	CM200S-32.768KDZB-UT	6pF	10pF	8 pF
Please work with your crystal vendor.				

EQUATION 9-1:

$$C_{load} = \frac{CX2 \times CX1}{CX2 + CX1} + C_{stray}$$

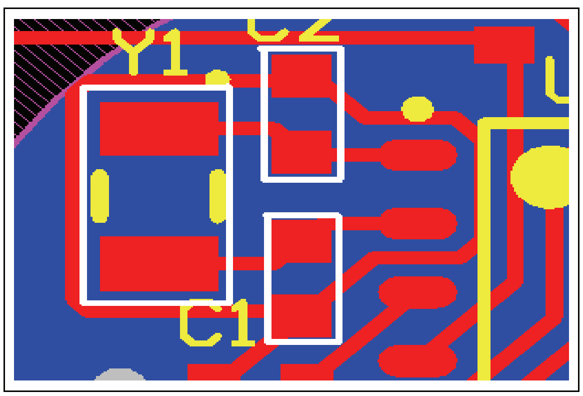
The following must also be taken into consideration:

- Pin capacitance (to be included in Cx2 and Cx1)
- Stray Board Capacitance

The recommended board layout for the oscillator area is shown in Figure 9-9. This actual board shows the crystal and the load capacitors. In this example, C2 is CX1, C1 is CX2 and the crystal is designated as Y1.

When calculating the effective load capacitance, Equation 9-1 can be used.

FIGURE 9-9: BOARD LAYOUT



Gerber files are available on request. Please contact your Microchip Sales representative.

It is required that the final application should be tested with the chosen crystal and capacitor combinations across all operating and environmental conditions. Please also consult with the crystal specification to observe correct handling and reflow conditions and for information on ideal capacitor values.

For more information please see the RTCC Best Practices AN1365 (DS01365).

10.0 ON-BOARD MEMORY

The MCP795XXX has both on-board EEPROM memory and battery-backed SRAM. The SRAM is arranged as 64 x 8 bytes and is retained when V_{CC} supply is removed. The EEPROM is organized as 256/128 x 8 bytes. The EEPROM is nonvolatile and does not require V_{BAT} supply for retention.

10.1 SRAM

The SRAM array is a battery-backed-up array of 64 bytes. The SRAM is accessed using the Read and Write commands, starting at address 0x20h.

Upon power-up the SRAM locations are in an undefined state but can be set to a known value using the `CLRRAM` instruction (Figure 9-8).

10.1.1 SRAM/RTCC OPERATION

The MCP795XXX contains a Real-Time Clock and Calendar. The RTCC registers and SRAM array are accessed using the same commands. The RTCC registers and SRAM array are powered internally from the switched supply that is either connected to V_{CC} or V_{BAT} supply. No external read/write operations are permitted when the device is running from the V_{BAT} supply.

Table 1-2 contains a list of the possible instruction bytes and format for device operation.

10.1.2 READ SEQUENCE

The part is selected by pulling $\overline{CS}$ low. The 8-bit `READ` instruction is transmitted to the MCP795W20 followed by the 8-bit address (A7 through A0). After the correct `READ` instruction and address are sent, the data stored in the memory at the selected address is shifted out on the SO pin. The data stored in the memory at the next address can be read sequentially by continuing to provide clock pulses. The internal Address Pointer is automatically incremented to the next higher address after each byte of data is shifted out.

As the RTCC registers are separate from the SRAM array, when reading the RTCC registers set the address will wrap back to the start of the RTCC registers. Also when an address within the SRAM array is loaded the internal Address Pointer will wrap back to the start of the SRAM array. The `READ` instruction can be used to read the registers and array indefinitely by continuing to clock the device. The read operation is terminated by raising the $\overline{CS}$ pin (Figure 10-1).

10.1.3 WRITE SEQUENCE

As the RTCC registers and SRAM array do not require the WREN sequence like the nonvolatile memory, the user may proceed by setting the $\overline{CS}$ low, issuing the WRITE instruction, followed by the address, and then the data to be written. As no write cycle is required for the RTCC registers and SRAM array the entire contents can be written in a single command.

For the last data byte to be written to the RTCC registers and SRAM array, the $\overline{CS}$ must be brought high after the last byte has been clocked in. If $\overline{CS}$ is brought high at any other time, the last byte will not be written. Refer to Figure 10-2 for more detailed illustrations on the write sequence.

FIGURE 10-1: READ SEQUENCE

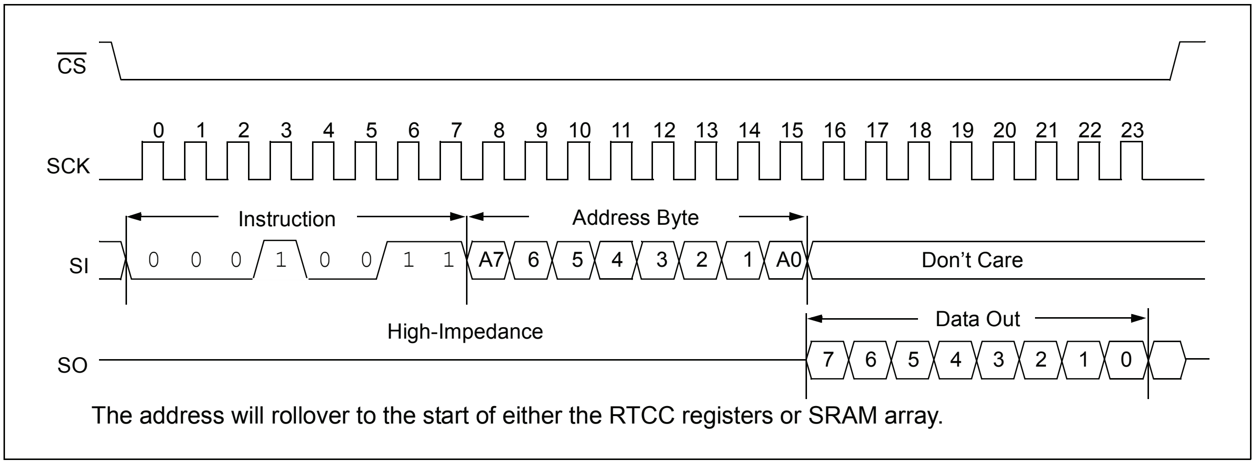
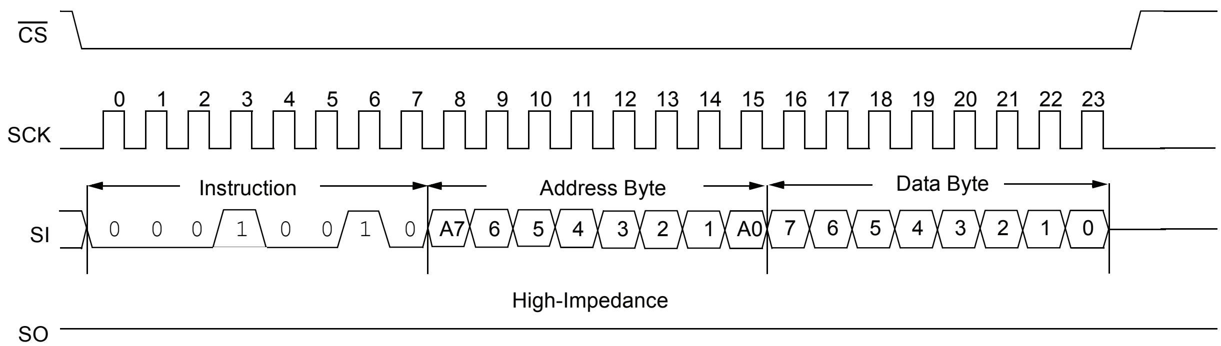


FIGURE 10-2: WRITE SEQUENCE



10.1.4 WRITE TO THE UNLOCK REGISTER

The MCP795XXX contains a protected area of 64 bits that can be used to hold a unique ID, such as a serial number or MAC address code. To gain write access to these locations, a specific sequence is required. Any deviation from this sequence will reset the lock on these locations. Once these locations have been unlocked they have to be written to in the next command by issuing the correct command. A write to a different location will lock the ID locations and clear the WEL bit.

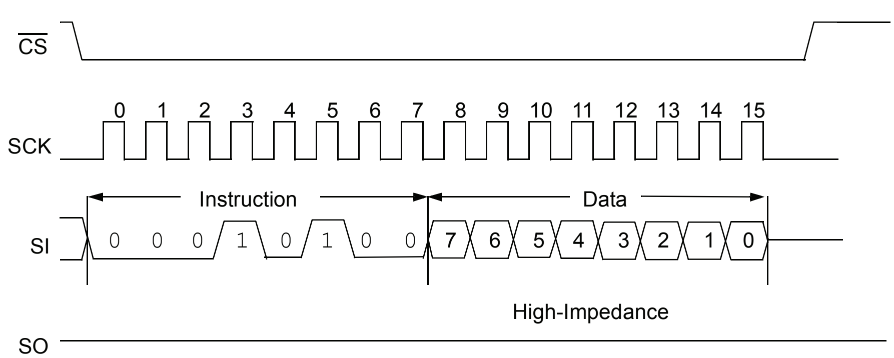
The following is a list of strict conditions which have to be followed before the unique locations can be written to:

- `EEWREN` instruction successfully executed
- `UNLOCK` 0x55 instruction successfully executed
- `UNLOCK` 0xAA instruction successfully executed

To issue each Unlock instruction the UNLOCK command is sent followed by 0x55. Then in a separate command the UNLOCK command is issued followed by 0xAA. It is a requirement that each command be separate, that is $\overline{\text{CS}}$ must toggle between each command.

Information on how to read and write the ID locations is detailed in Section 9.1.6, Unique ID Locations.

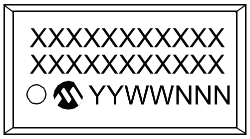
FIGURE 10-3: UNLOCK SEQUENCE



11.0 PACKAGING INFORMATION

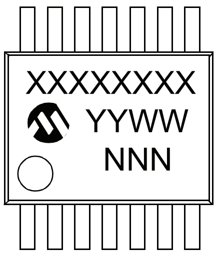
11.1 Package Marking Information

14-Lead SOIC (.150”)

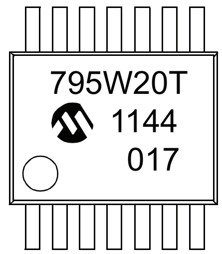


Example

14-Lead TSSOP



Example



Part Number	1st Line Marking Codes	
	SOIC	TSSOP
MCP795W20	MCP795W20	795W20T
MCP795W10	MCP795W10	795W10T
MCP795W21	MCP795W21	795W21T
MCP795W11	MCP795W11	795W11T
MCP795W22	MCP795W22	795W22T
MCP795W12	MCP795W12	795W12T
MCP795B20	MCP795B20	795B20T
MCP795B10	MCP795B10	795B10T
MCP795B21	MCP795B21	795B21T
MCP795B11	MCP795B11	795B11T
MCP795B22	MCP795B22	795B22T
MCP795B12	MCP795B12	795B12T

Note: T = Temperature grade
NN = Alphanumeric traceability code

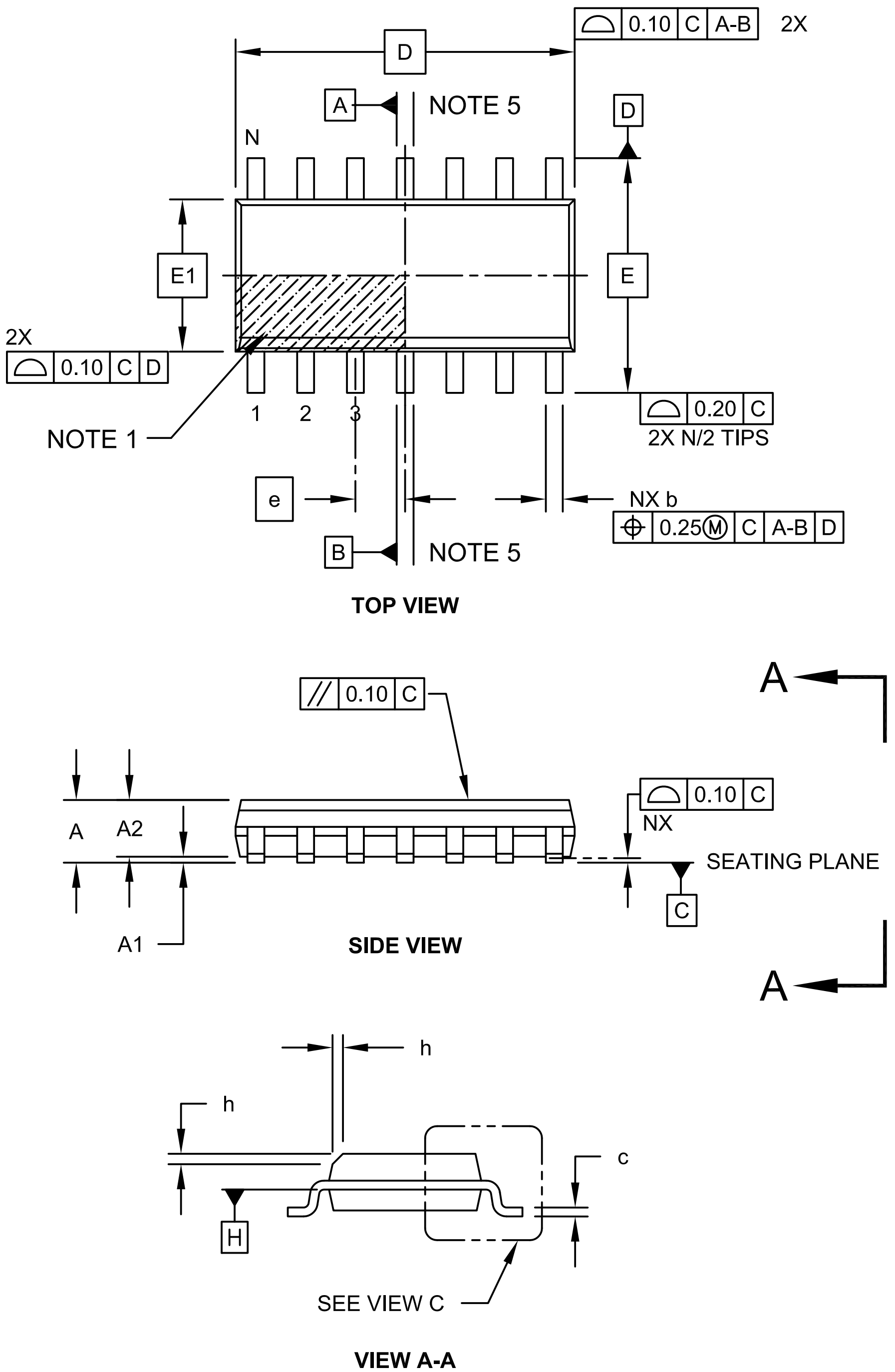
Legend:

XX...X	Customer-specific information
Y	Year code (last digit of calendar year)
YY	Year code (last 2 digits of calendar year)
WW	Week code (week of January 1 is week ‘01’)
NNN	Alphanumeric traceability code
e3	Pb-free JEDEC designator for Matte Tin (Sn)
*	This package is Pb-free. The Pb-free JEDEC designator (e3) can be found on the outer packaging for this package.

Note: In the event the full Microchip part number cannot be marked on one line, it will be carried over to the next line, thus limiting the number of available characters for customer-specific information.

14-Lead Plastic Small Outline (SL) - Narrow, 3.90 mm Body [SOIC]

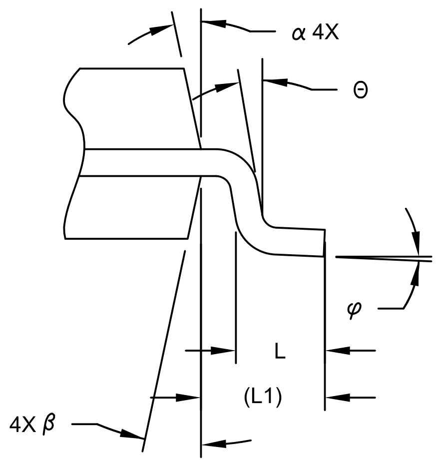
Note:	For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



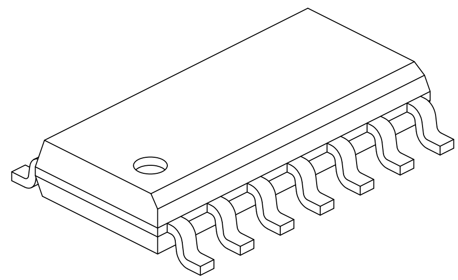
Microchip Technology Drawing No. C04-065C Sheet 1 of 2

14-Lead Plastic Small Outline (SL) - Narrow, 3.90 mm Body [SOIC]

Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



VIEW C



		Units	MILLIMETERS		
Dimension Limits			MIN	NOM	MAX
Number of Pins		N		14	
Pitch		e		1.27 BSC	
Overall Height		A	-	-	1.75
Molded Package Thickness		A2	1.25	-	-
Standoff	§	A1	0.10	-	0.25
Overall Width		E		6.00 BSC	
Molded Package Width		E1		3.90 BSC	
Overall Length		D		8.65 BSC	
Chamfer (Optional)		h	0.25	-	0.50
Foot Length		L	0.40	-	1.27
Footprint		L1		1.04 REF	
Lead Angle		Θ	0°	-	-
Foot Angle		φ	0°	-	8°
Lead Thickness		c	0.10	-	0.25
Lead Width		b	0.31	-	0.51
Mold Draft Angle Top		α	5°	-	15°
Mold Draft Angle Bottom		β	5°	-	15°

Notes:

1. Pin 1 visual index feature may vary, but must be located within the hatched area.
2. § Significant Characteristic
3. Dimension D does not include mold flash, protrusions or gate burrs, which shall not exceed 0.15 mm per end. Dimension E1 does not include interlead flash or protrusion, which shall not exceed 0.25 mm per side.
4. Dimensioning and tolerancing per ASME Y14.5M

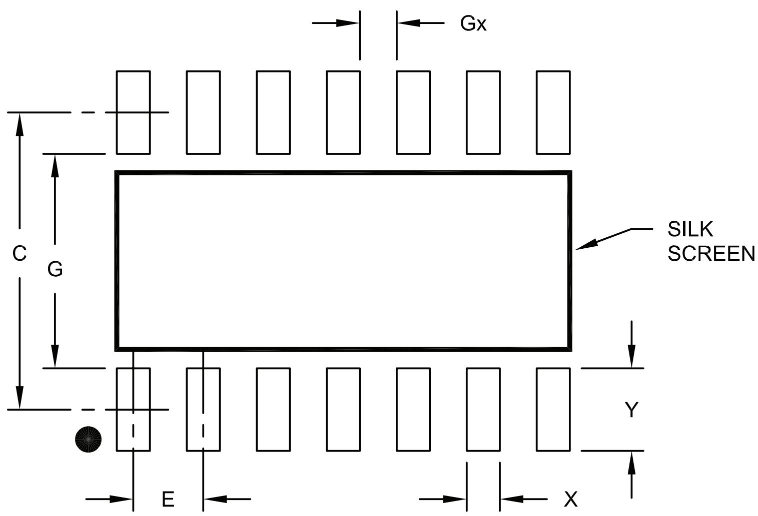
   BSC: Basic Dimension. Theoretically exact value shown without tolerances.

   REF: Reference Dimension, usually without tolerance, for information purposes only.
5. Datums A & B to be determined at Datum H.

Microchip Technology Drawing No. C04-065C Sheet 2 of 2

14-Lead Plastic Small Outline (SL) - Narrow, 3.90 mm Body [SOIC]

Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



RECOMMENDED LAND PATTERN

Units		MILLIMETERS		
Dimension Limits		MIN	NOM	MAX
Contact Pitch	E	1.27 BSC		
Contact Pad Spacing	C		5.40	
Contact Pad Width	X			0.60
Contact Pad Length	Y			1.50
Distance Between Pads	Gx	0.67		
Distance Between Pads	G	3.90		

Notes:

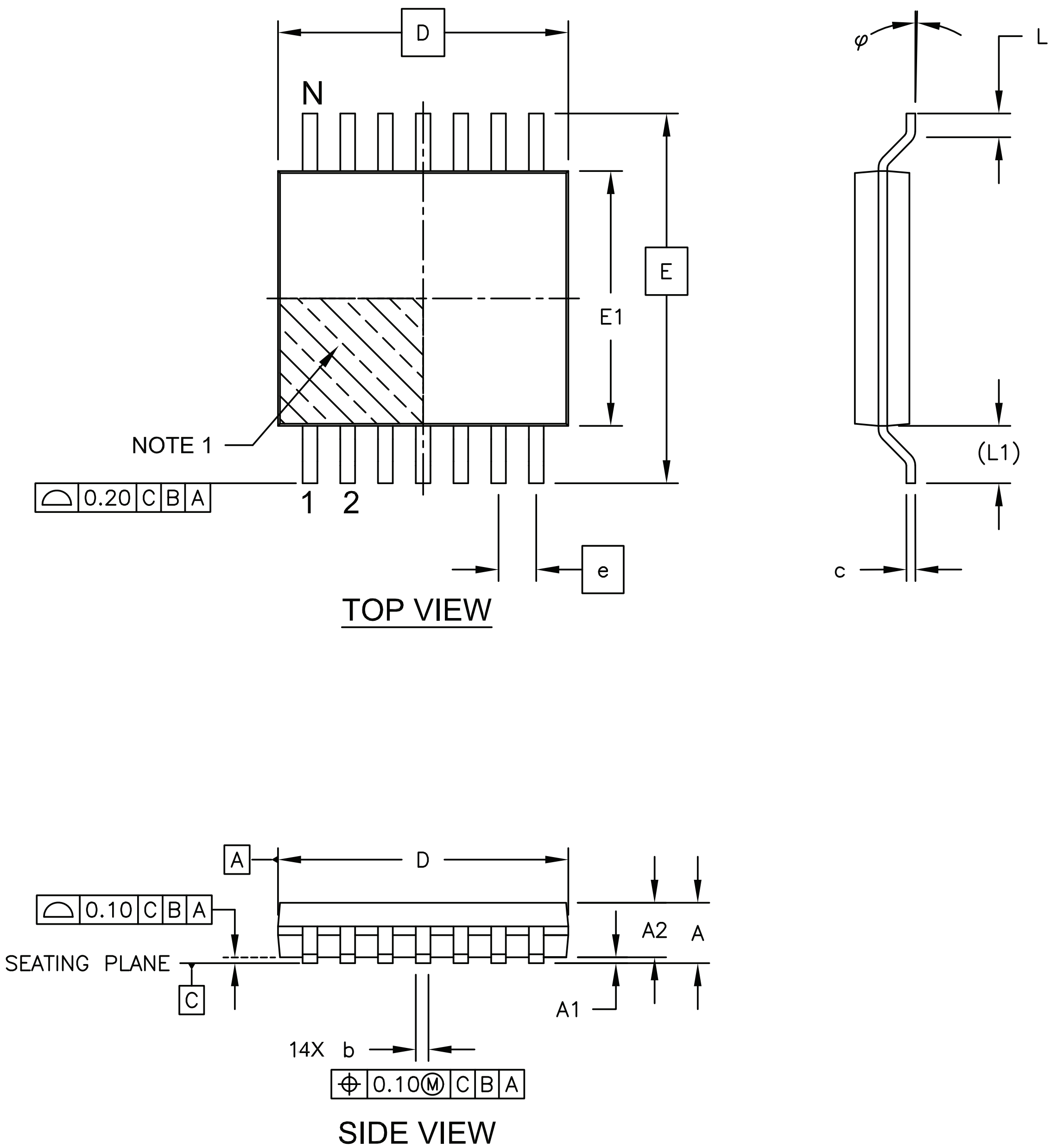
1. Dimensioning and tolerancing per ASME Y14.5M

BSC: Basic Dimension. Theoretically exact value shown without tolerances.

Microchip Technology Drawing No. C04-2065A

14-Lead Plastic Thin Shrink Small Outline (ST) - 4.4 mm Body [TSSOP]

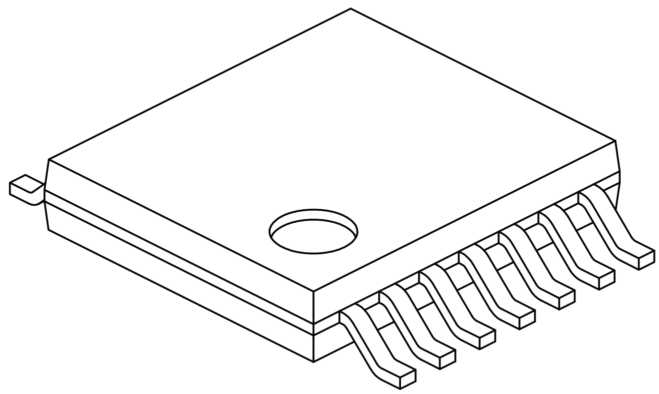
Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



Microchip Technology Drawing C04-087C Sheet 1 of 2

14-Lead Plastic Thin Shrink Small Outline (ST) - 4.4 mm Body [TSSOP]

Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



	Units	MILLIMETERS		
	Dimension Limits	MIN	NOM	MAX
Number of Pins	N		14	
Pitch	e		0.65 BSC	
Overall Height	A	-	-	1.20
Molded Package Thickness	A2	0.80	1.00	1.05
Standoff	A1	0.05	-	0.15
Overall Width	E		6.40 BSC	
Molded Package Width	E1	4.30	4.40	4.50
Molded Package Length	D	4.90	5.00	5.10
Foot Length	L	0.45	0.60	0.75
Footprint	(L1)		1.00 REF	
Foot Angle	φ	0°	-	8°
Lead Thickness	c	0.09	-	0.20
Lead Width	b	0.19	-	0.30

Notes:

1. Pin 1 visual index feature may vary, but must be located within the hatched area.
2. Dimensions D and E1 do not include mold flash or protrusions. Mold flash or protrusions shall not exceed 0.15mm per side.
3. Dimensioning and tolerancing per ASME Y14.5M

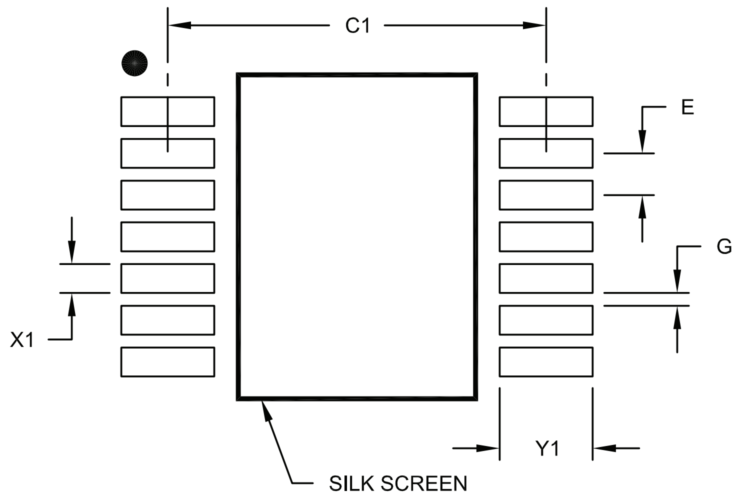
   BSC: Basic Dimension. Theoretically exact value shown without tolerances.

   REF: Reference Dimension, usually without tolerance, for information purposes only.

Microchip Technology Drawing No. C04-087C Sheet 2 of 2

14-Lead Plastic Thin Shrink Small Outline (ST) - 4.4 mm Body [TSSOP]

Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



RECOMMENDED LAND PATTERN

Units		MILLIMETERS		
Dimension Limits		MIN	NOM	MAX
Contact Pitch	E	0.65 BSC		
Contact Pad Spacing	C1		5.90	
Contact Pad Width (X14)	X1			0.45
Contact Pad Length (X14)	Y1			1.45
Distance Between Pads	G	0.20		

Notes:

1. Dimensioning and tolerancing per ASME Y14.5M

   BSC: Basic Dimension. Theoretically exact value shown without tolerances.

Microchip Technology Drawing No. C04-2087A

 Preliminary

APPENDIX A: REVISION HISTORY

Revision A (11/2011)

Initial Release.

NOTES:

THE MICROCHIP WEB SITE

Microchip provides online support via our WWW site at www.microchip.com. This web site is used as a means to make files and information easily available to customers. Accessible by using your favorite Internet browser, the web site contains the following information:

- **Product Support** – Data sheets and errata, application notes and sample programs, design resources, user's guides and hardware support documents, latest software releases and archived software
- **General Technical Support** – Frequently Asked Questions (FAQ), technical support requests, online discussion groups, Microchip consultant program member listing
- **Business of Microchip** – Product selector and ordering guides, latest Microchip press releases, listing of seminars and events, listings of Microchip sales offices, distributors and factory representatives

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- Distributor or Representative
- Local Sales Office
- Field Application Engineer (FAE)
- Technical Support
- Development Systems Information Line

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It is our intention to provide you with the best documentation possible to ensure successful use of your Microchip product. If you wish to provide your comments on organization, clarity, subject matter, and ways in which our documentation can better serve you, please FAX your comments to the Technical Publications Manager at (480) 792-4150.

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Device: MCP795WXX/MCP795BXX Literature Number: DS22280A

Questions:

1. What are the best features of this document?

____

____

2. How does this document meet your hardware and software development needs?

____

____

3. Do you find the organization of this document easy to follow? If not, why?

____

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4. What additions to the document do you think would enhance the structure and subject?

____

____

5. What deletions from the document could be made without affecting the overall usefulness?

____

____

6. Is there any incorrect or misleading information (what and where)?

____

____

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____

____

PRODUCT IDENTIFICATION SYSTEM

To order or obtain information, e.g., on pricing or delivery, refer to the factory or the listed sales office. Not every possible ordering combination is listed below.

MCP795	W	1	0	T	– I	/SN
Base Part	Additional Features	Memory	Unique ID	T/R	Temp Range	Package

Base Part No.:	MCP794	=	I^2C™ RTCC
	MCP795	=	SPI RTCC
Additional Features:	Blank	=	None
	W	=	Watchdog Timer, 2 Event Detects
	B	=	32 kHz Boot-up Clock, Watchdog Timer, 2 Event Detects
Memory:	0	=	64 Bytes SRAM
	1	=	1 Kbit EE, 64 Bytes SRAM
	2	=	2 Kbits EE, 64 Bytes SRAM
ID/MAC Address:	0	=	Blank
	1	=	EUI-48™ MAC Address
	2	=	EUI-64™ MAC Address
T/R:	Blank	=	Tube
	T	=	Tape and Reel
Temperature Range:	I	=	-40°C to +85°C
Package:	SL	=	14-Pin SOIC
	ST	=	14-Pin TSSOP

Examples:

a) MCP795W20-I/SL: 2K EEPROM, Blank ID, Industrial Temperature, SOIC Package

b) MCP795W10-I/ST: 1K EEPROM, Blank ID, Industrial Temperature, TSSOP Package

c) MCP795W21-I/SL: 2K EEPROM, EUI-48™, Industrial Temperature, SOIC Package

d) MCP795W22-I/ST: 2K EEPROM, EUI-64™, Industrial Temperature, TSSOP Package

e) MCP795B20-I/SL: Boot Clock, 2K EEPROM, Blank ID, Industrial Temperature, SOIC Package

f) MCP795B10-I/ST: Boot Clock, 1K EEPROM, Blank ID, Industrial Temperature, TSSOP Package

Note 1: All devices include a Watchdog Timer and two Event Detects.

NOTES:

Note the following details of the code protection feature on Microchip devices:

- Microchip products meet the specification contained in their particular Microchip Data Sheet.
- Microchip believes that its family of products is one of the most secure families of its kind on the market today, when used in the intended manner and under normal conditions.
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